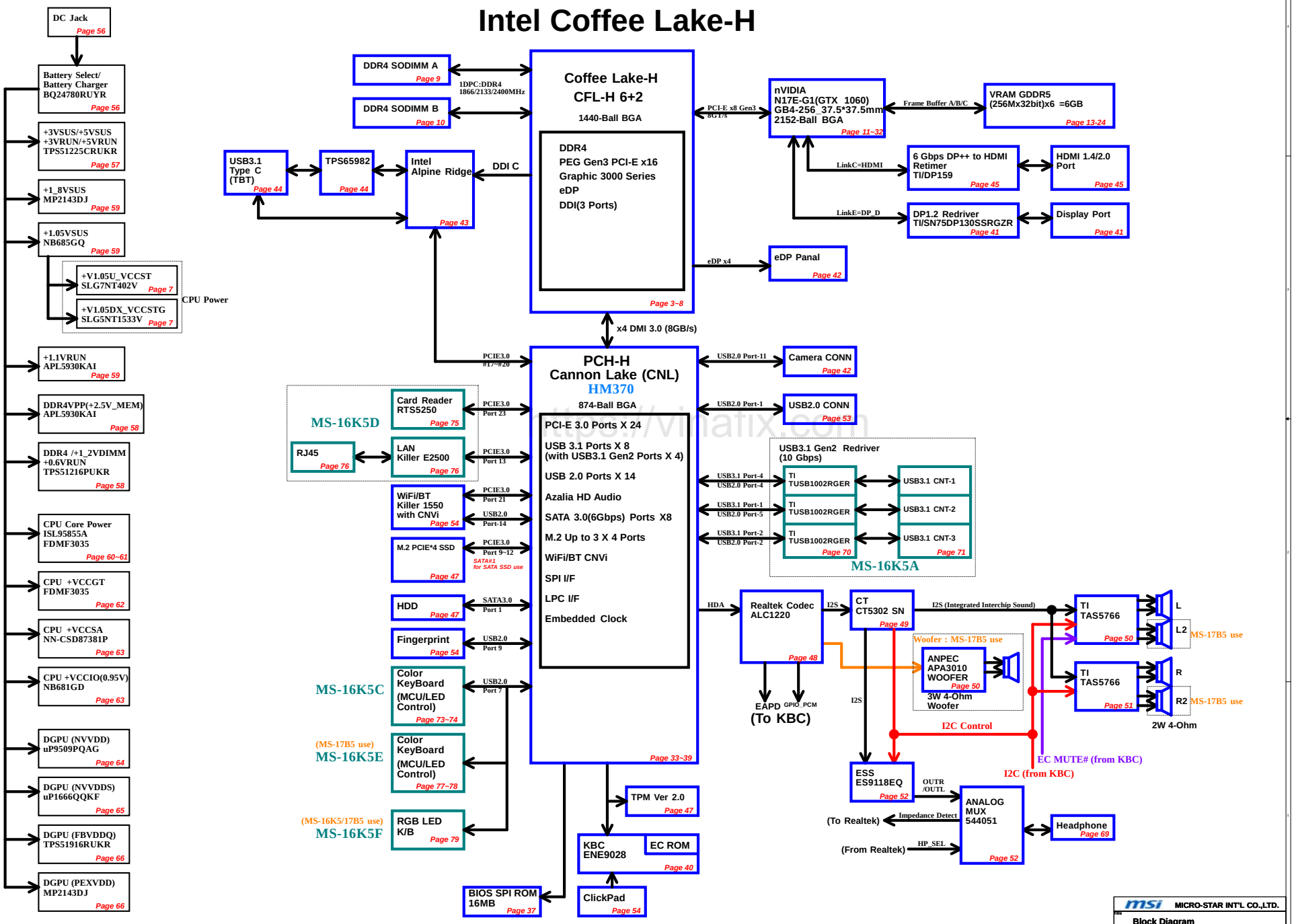
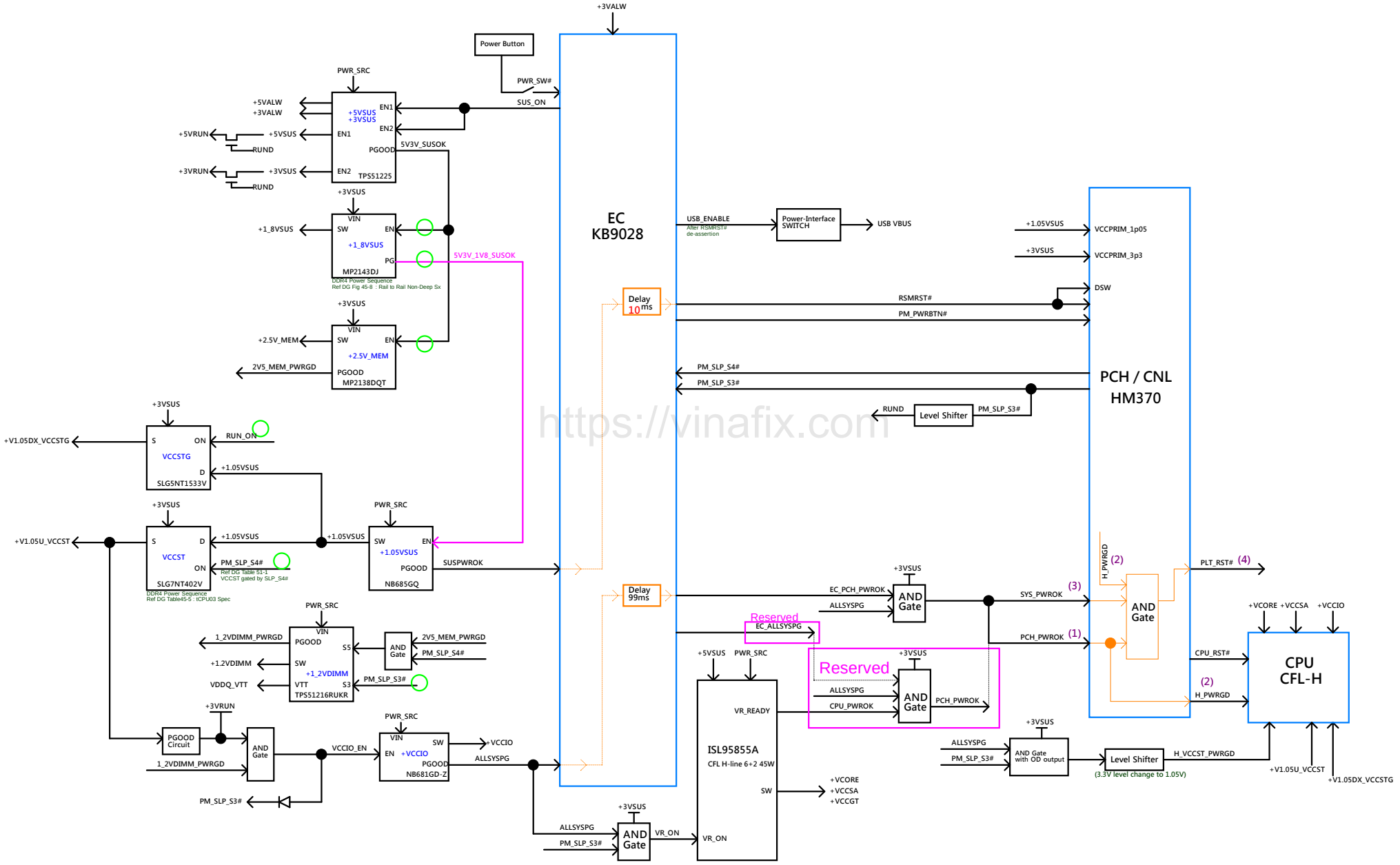
# MS-16K5/17B5 Ver : 0B



# MS-16K5 : CFL-H Mobile Power on Block Diagram

ref DG Chapter45 Power Sequencing Spec

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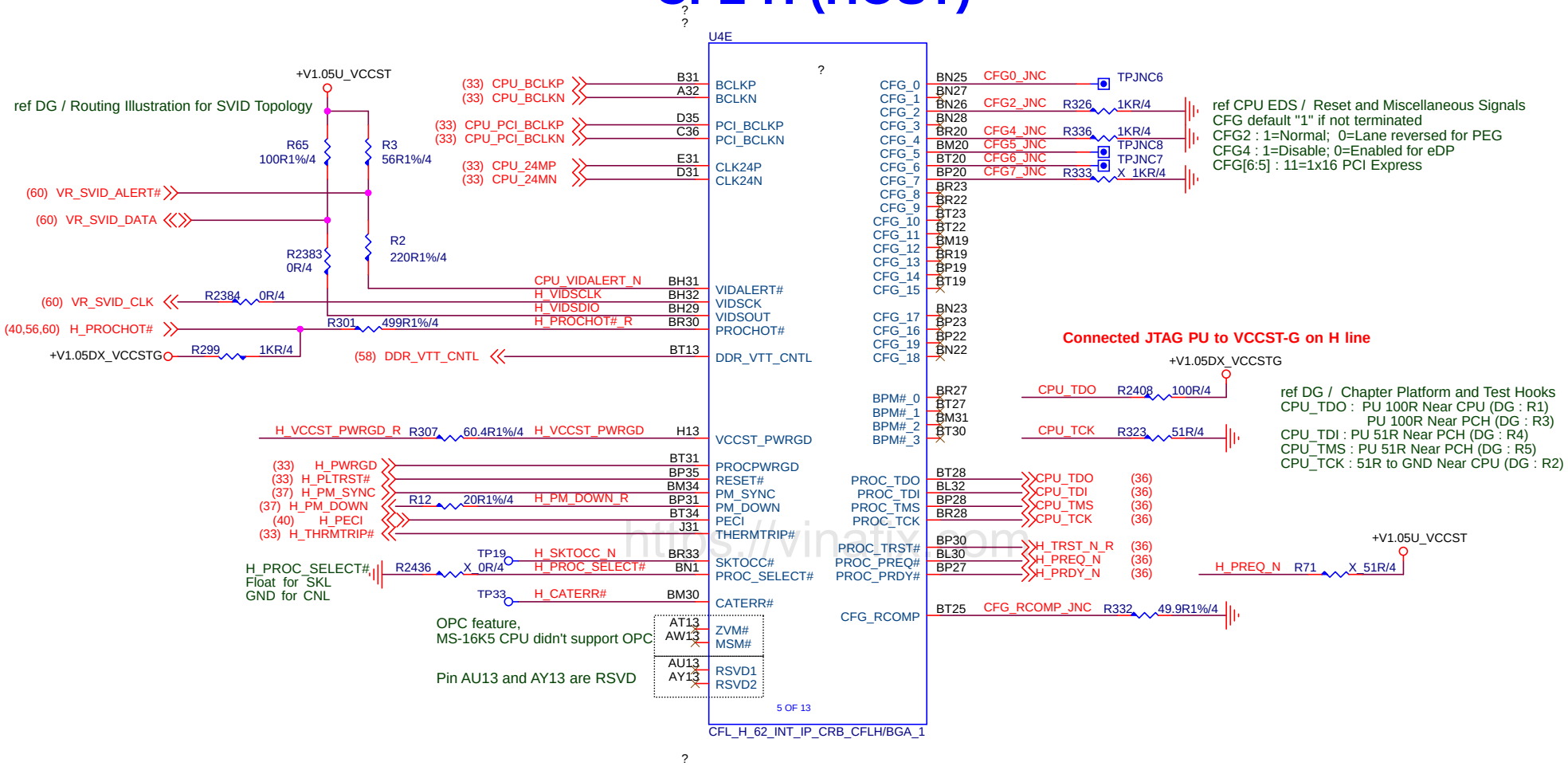
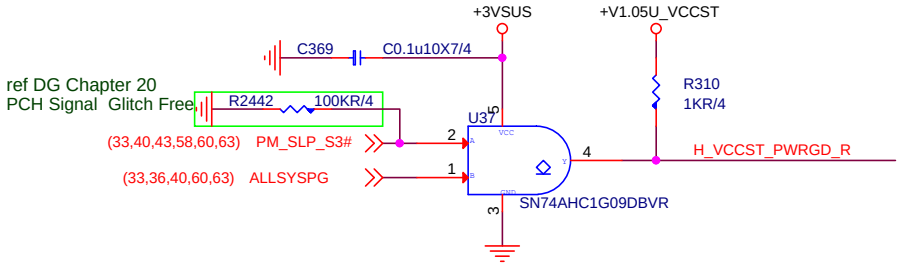
| | | | |
|---|---|---|---|
| Title | Power ON Block Diagram | | |
| Size | Document Number | | Rev |
| Custom | MS-16K5 | | 0B |
| Date: | Friday, October 06, 2017 | Sheet 2 of 80 | |

# CFL-H (HOST)



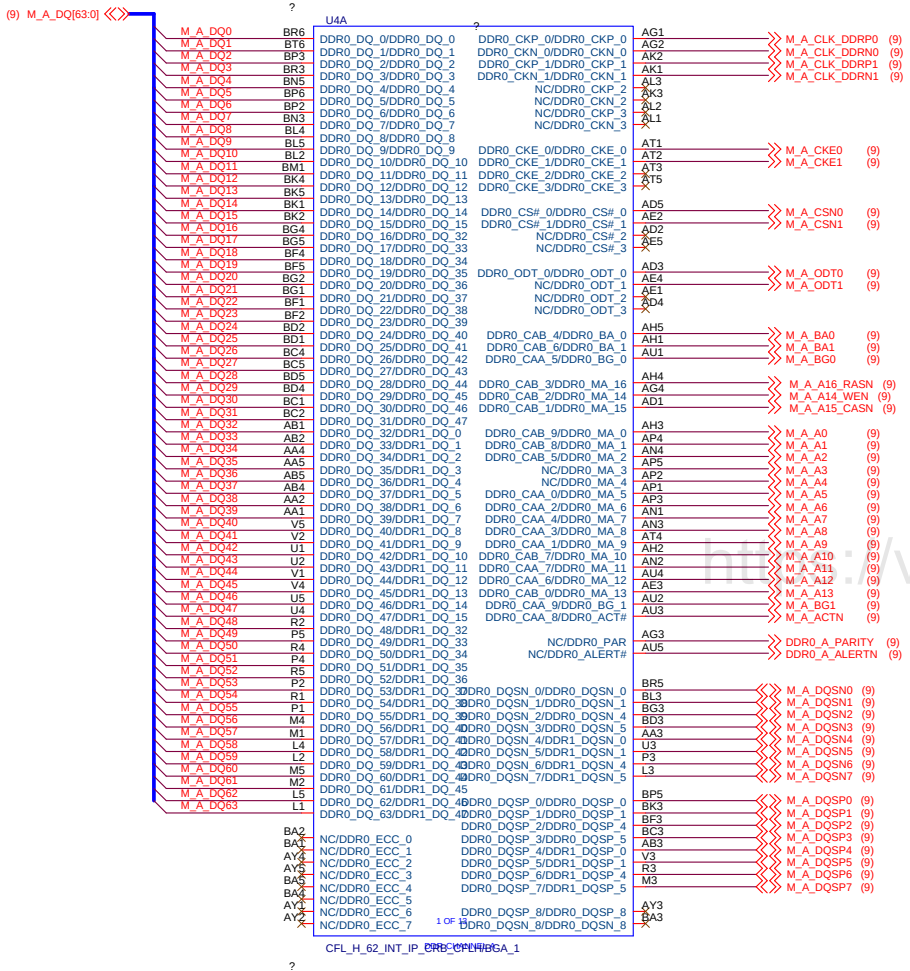

## VCCST_PWRGD
### (Level Shifter 3.3V to 1.05V)



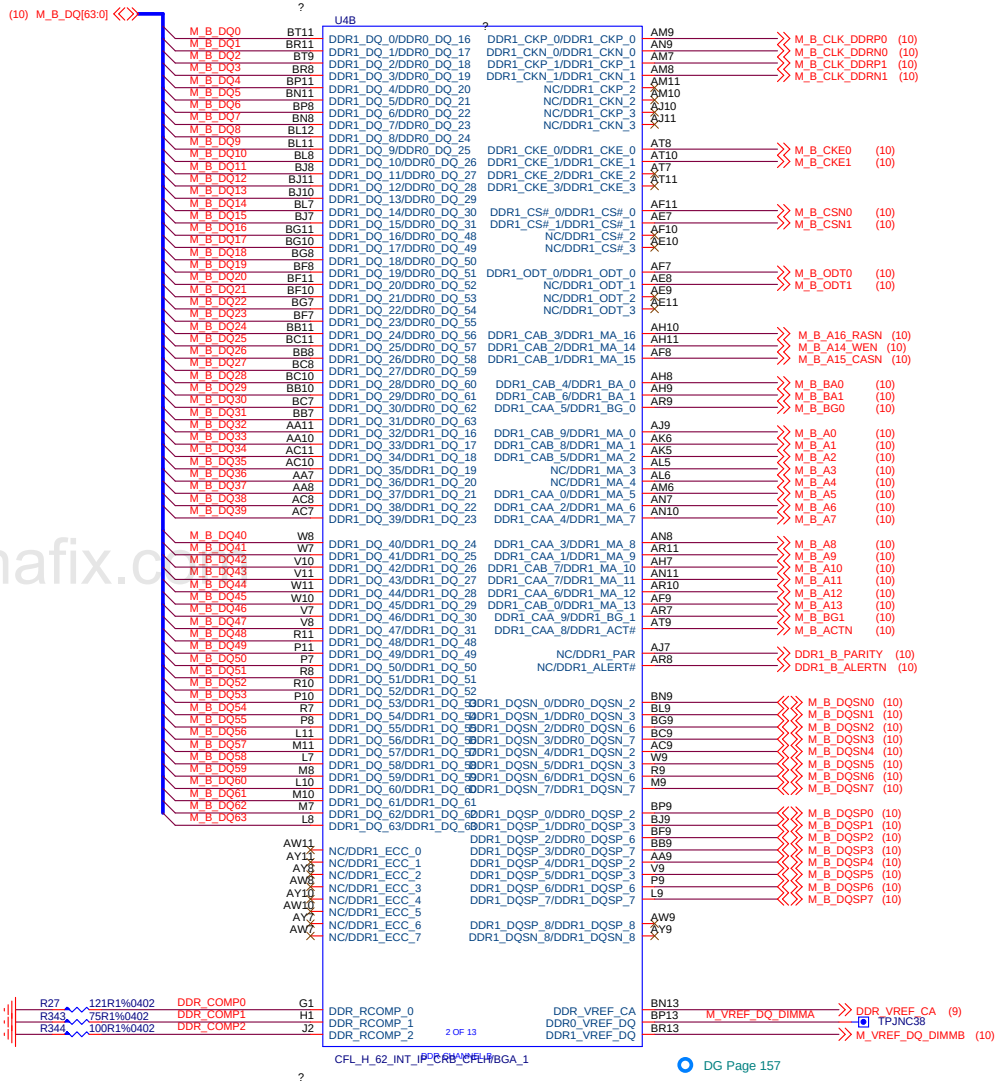

74AHC1G09GV is AND Gate with open drain output

| | | | |
|---|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | | |
| Title: CFL-H(HOST) | | | |
| Size: Custom | Document Number: MS-16K51 | | Rev: 0B |
| Date: Friday, October 06, 2017 | | Sheet 3 of 80 | |

# DDR Channel A




# DDR Channel B

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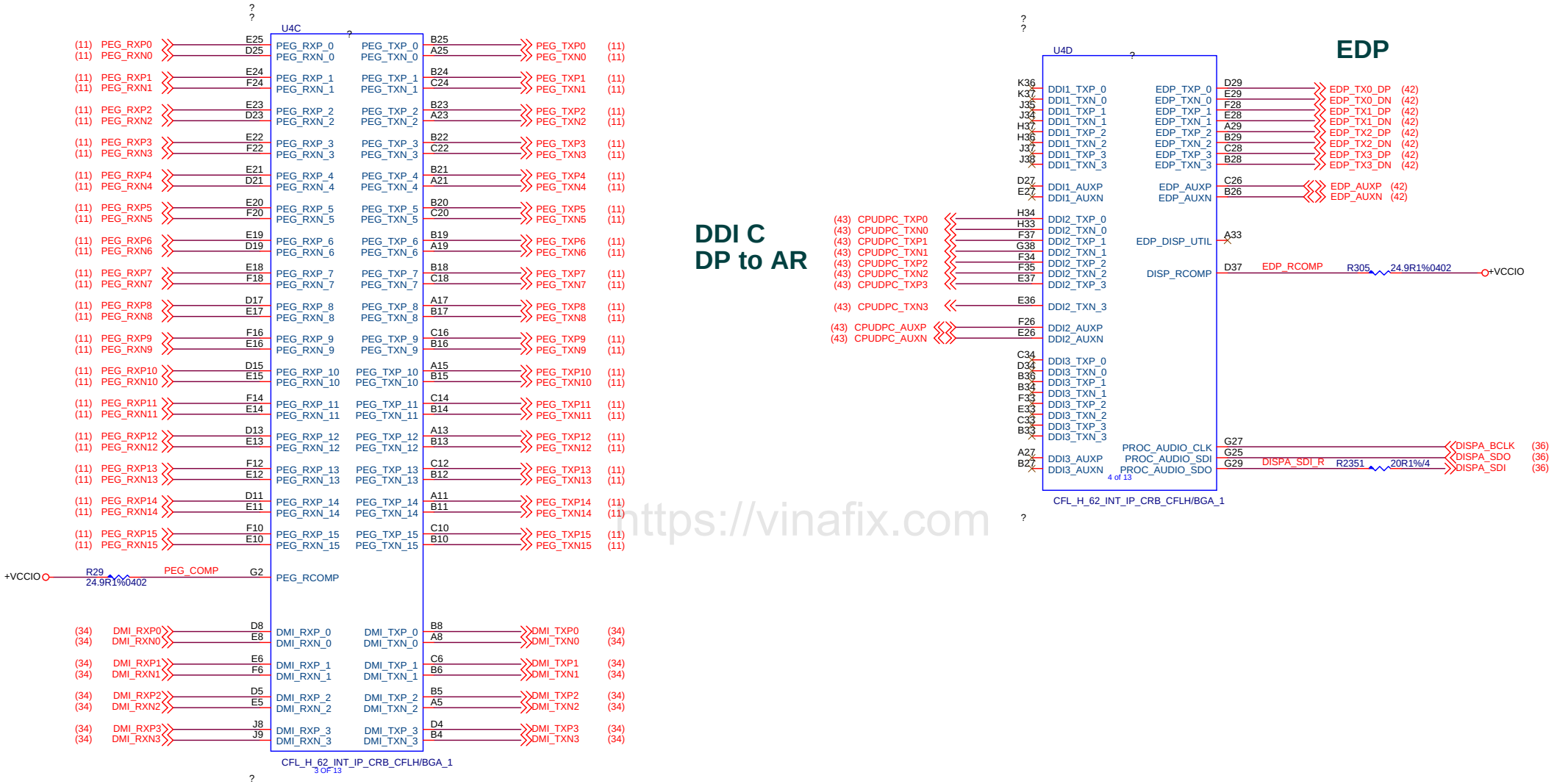
| | | | |
|---|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | | |
| Title: CFL-H(DDR4) | | | |
| Size: Custom | Document Number: MS-16K51 | | Rev: 0B |
| Date: Thursday, October 05, 2017 | Sheet 4 of 80 | | |

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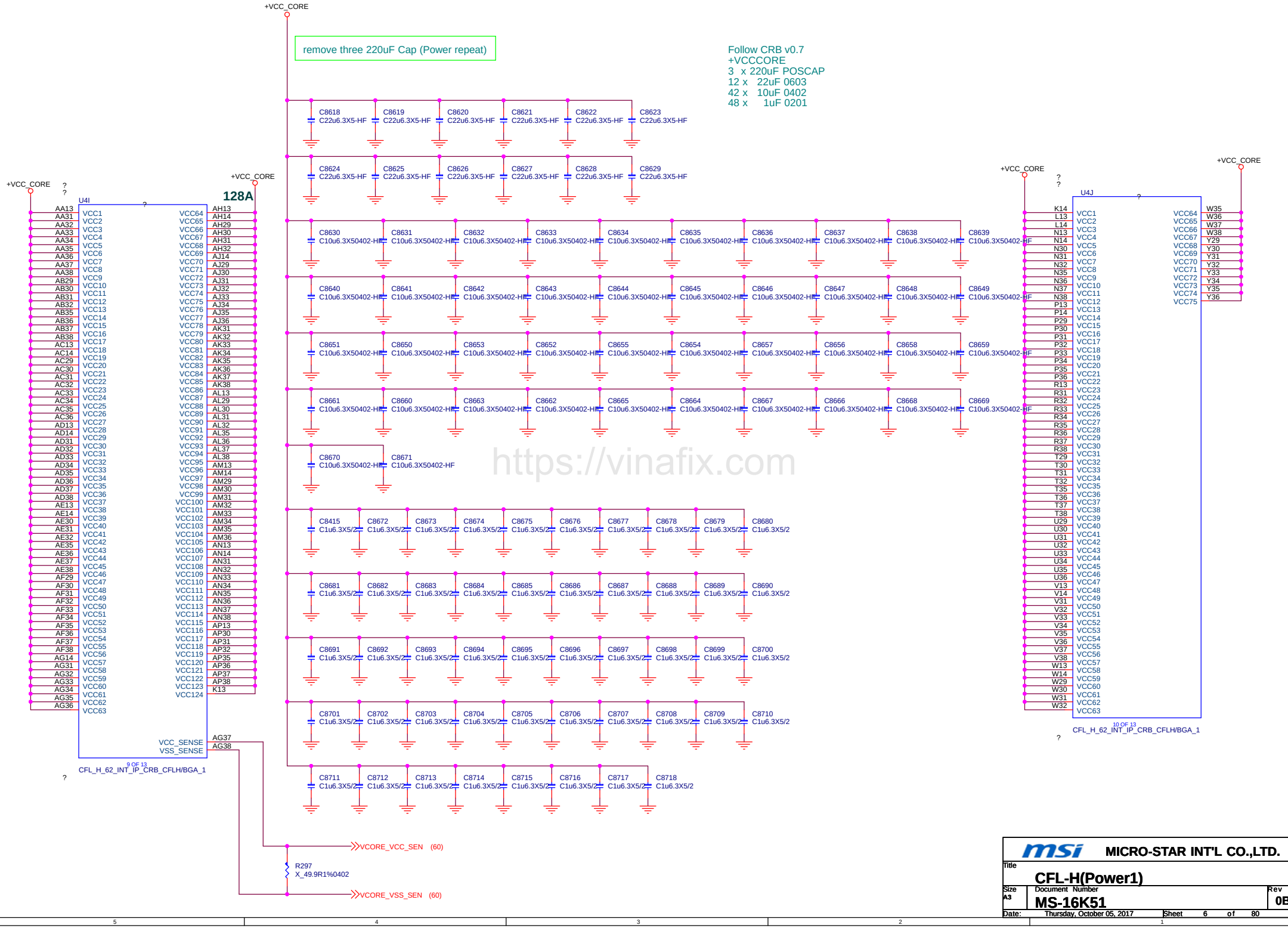
| | | |
|---|---|---|
| Title | CFL-H(DMI/Display) | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B |
| Date: Thursday, October 05, 2017 | Sheet 5 of 80 | |

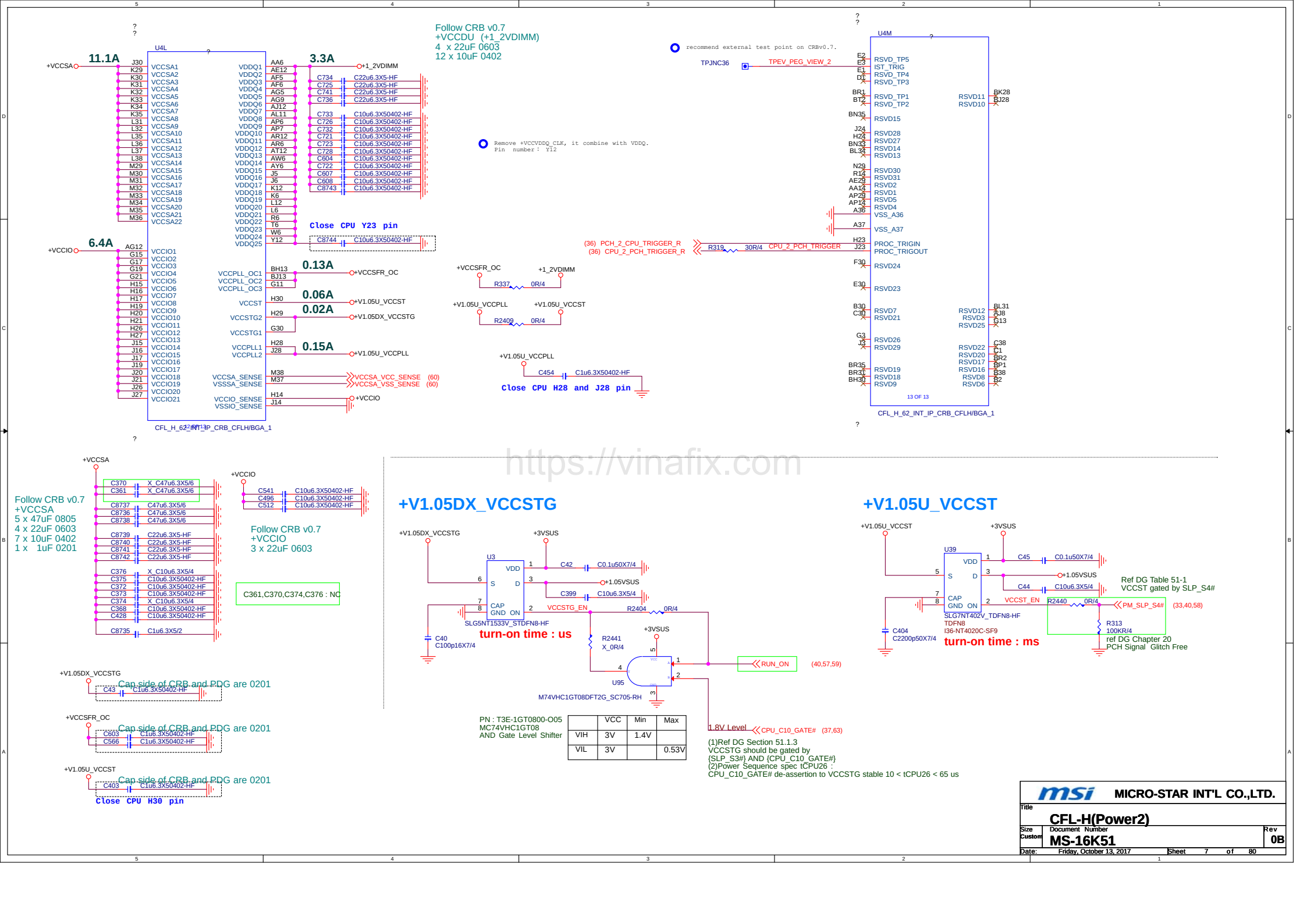



MICRO-STAR INT'L CO.,LTD.

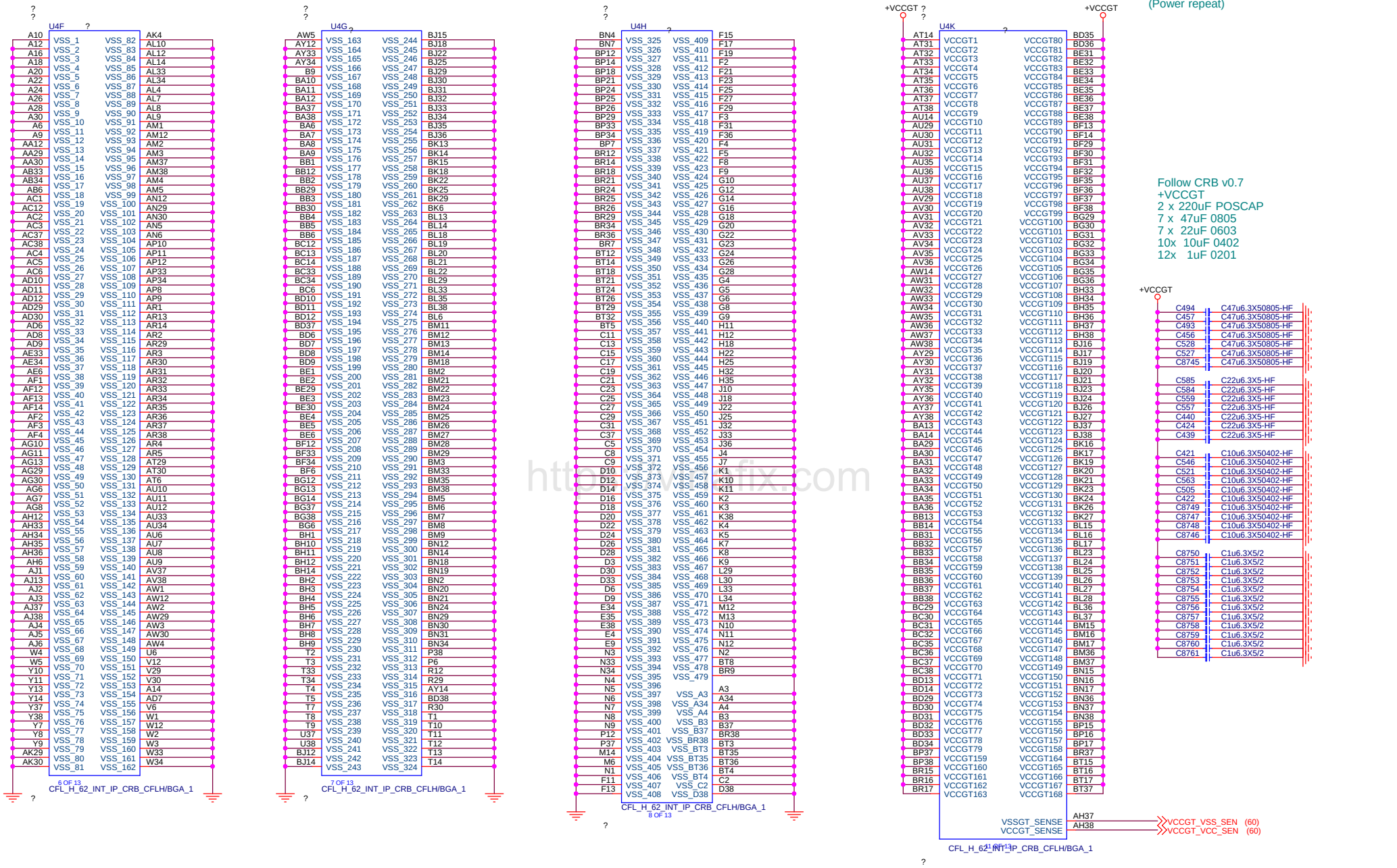
Title: CFL-H(Power1)

Size: A3 | Document Number: MS-16K51 | Rev: 0B

Date: Thursday, October 05, 2017 | Sheet 6 of 80




https://vinafix.com

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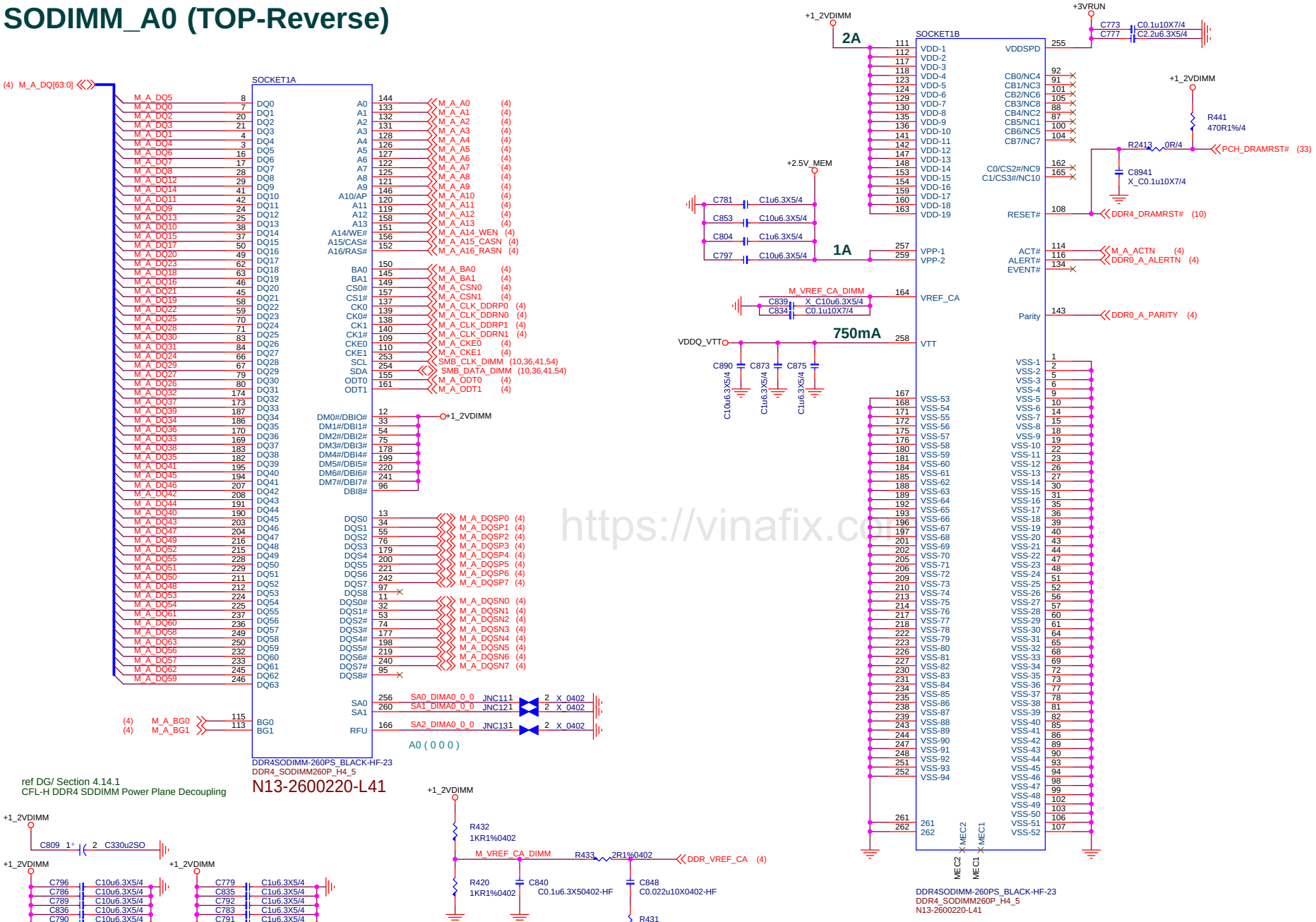
MICRO-STAR INT'L CO.,LTD.

Title: CFL-H(Power3)

Size: A3 | Document Number: MS-16K51 | Rev: 0B

Date: Thursday, October 05, 2017 | Sheet 8 of 80

# SODIMM_A0 (TOP-Reverse)

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| | |
|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD. |
| Title | DDR4_SODIMM_A0 |
| Size / Custom | Document Number: MS-16K51 |
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| Date: | Thursday, October 05, 2017 |
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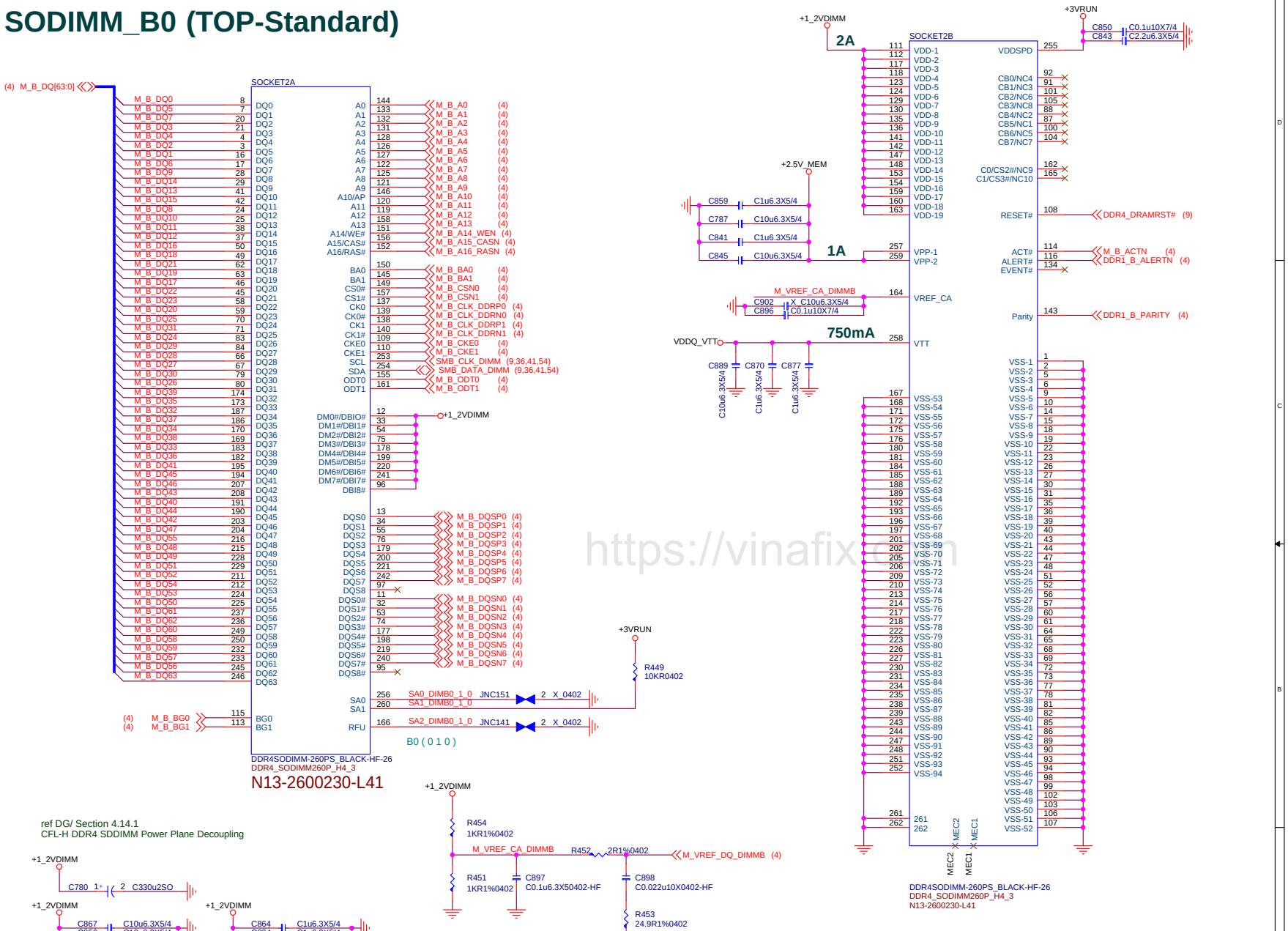
# SODIMM_B0 (TOP-Standard)

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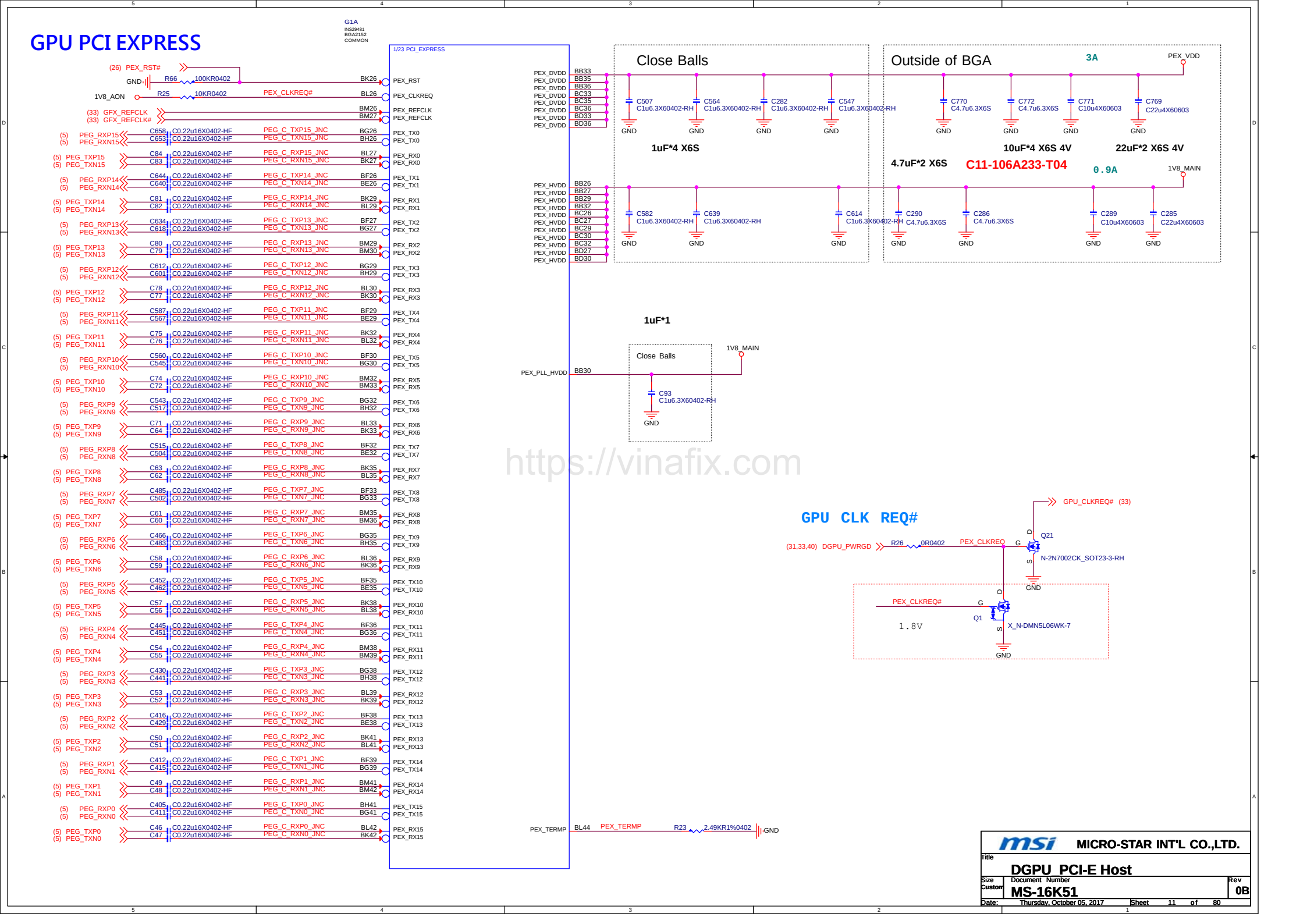
| | | |
|---|---|---|
| msi | MICRO-STAR INT'L CO.,LTD. | |
| Title | DDR4_SODIMM_B0 | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B |
| Date: Thursday, October 05, 2017 | Sheet 10 of 80 | |

# GPU PCI EXPRESS

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| | |
|---|---|
| Title | DGPU_PCI-E Host |
| Size | Custom |
| Document Number | MS-16K51 |
| Rev | 0B |
| Date | Thursday, October 05, 2017 |
| Sheet | 11 of 80 |

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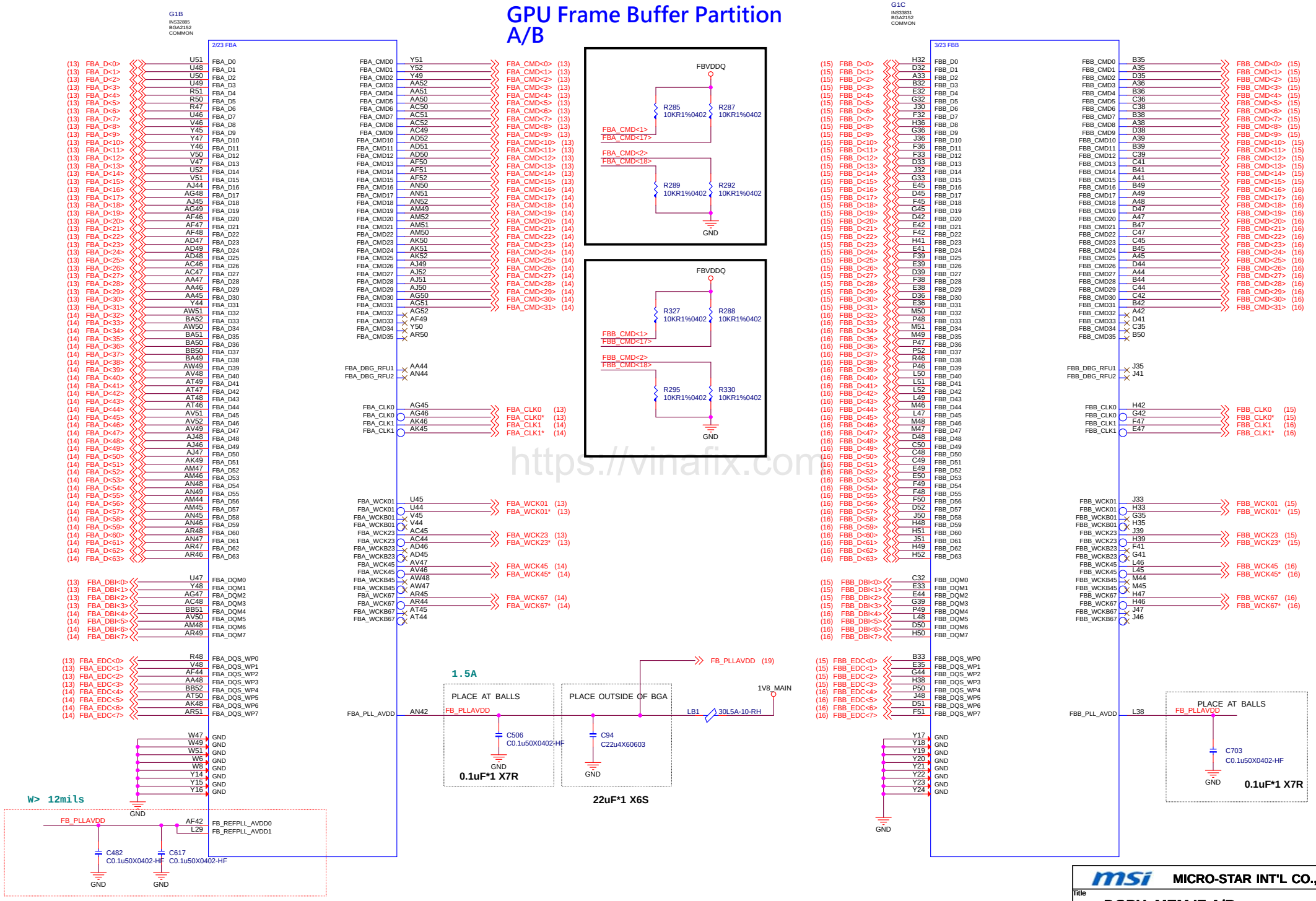
# GPU Frame Buffer Partition A/B

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| | |
|---|---|
| Title | DGPU_MEM IF A/B |
| Size | Custom |
| Document Number | MS-16K51 |
| Rev | 0B |
| Date: | Thursday, October 05, 2017 |
| Sheet | 12 of 80 |

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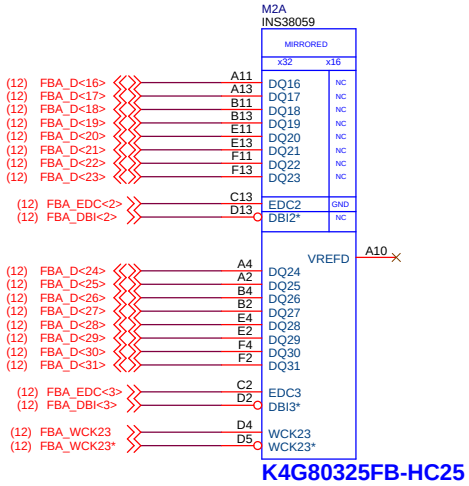
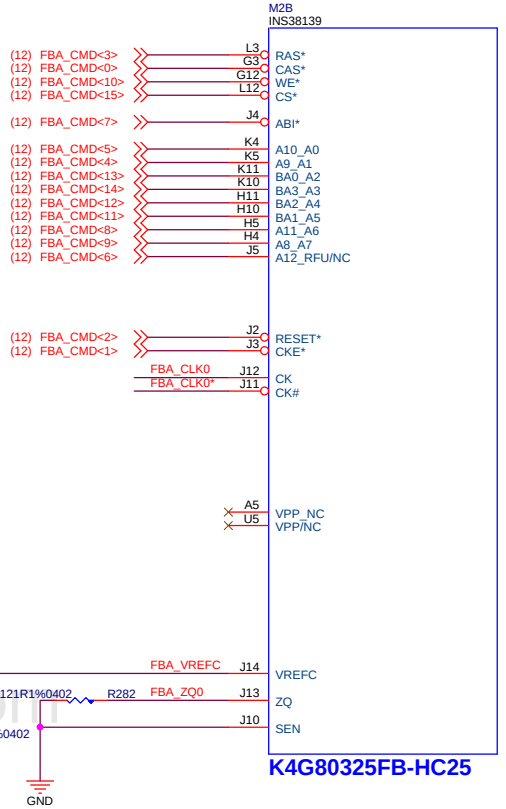
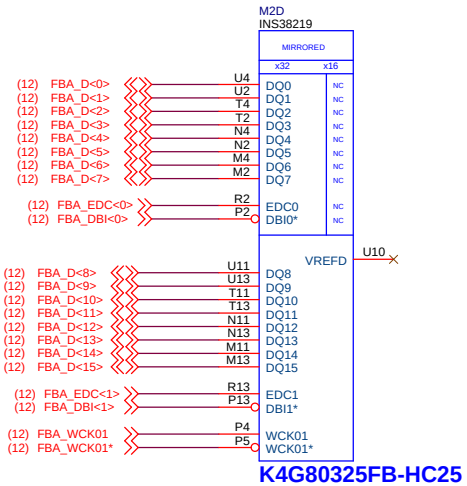
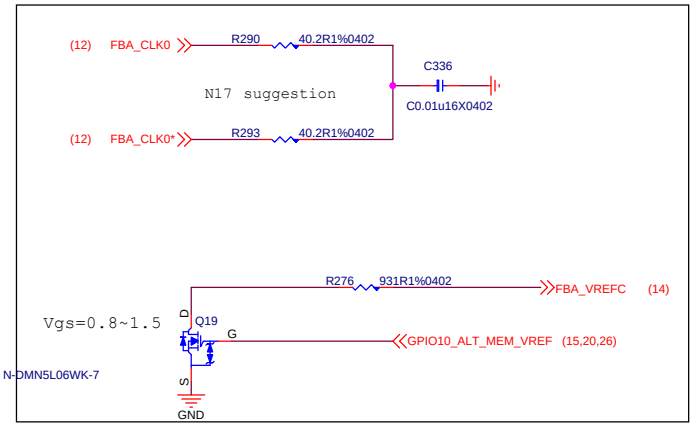
# DGPU_GDDR5 FrameBuffer A0

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Title: DGPU_GDDR5 FrameBuffer A0

Size: A3 | Document Number: MS-16K51 | Rev: 0B

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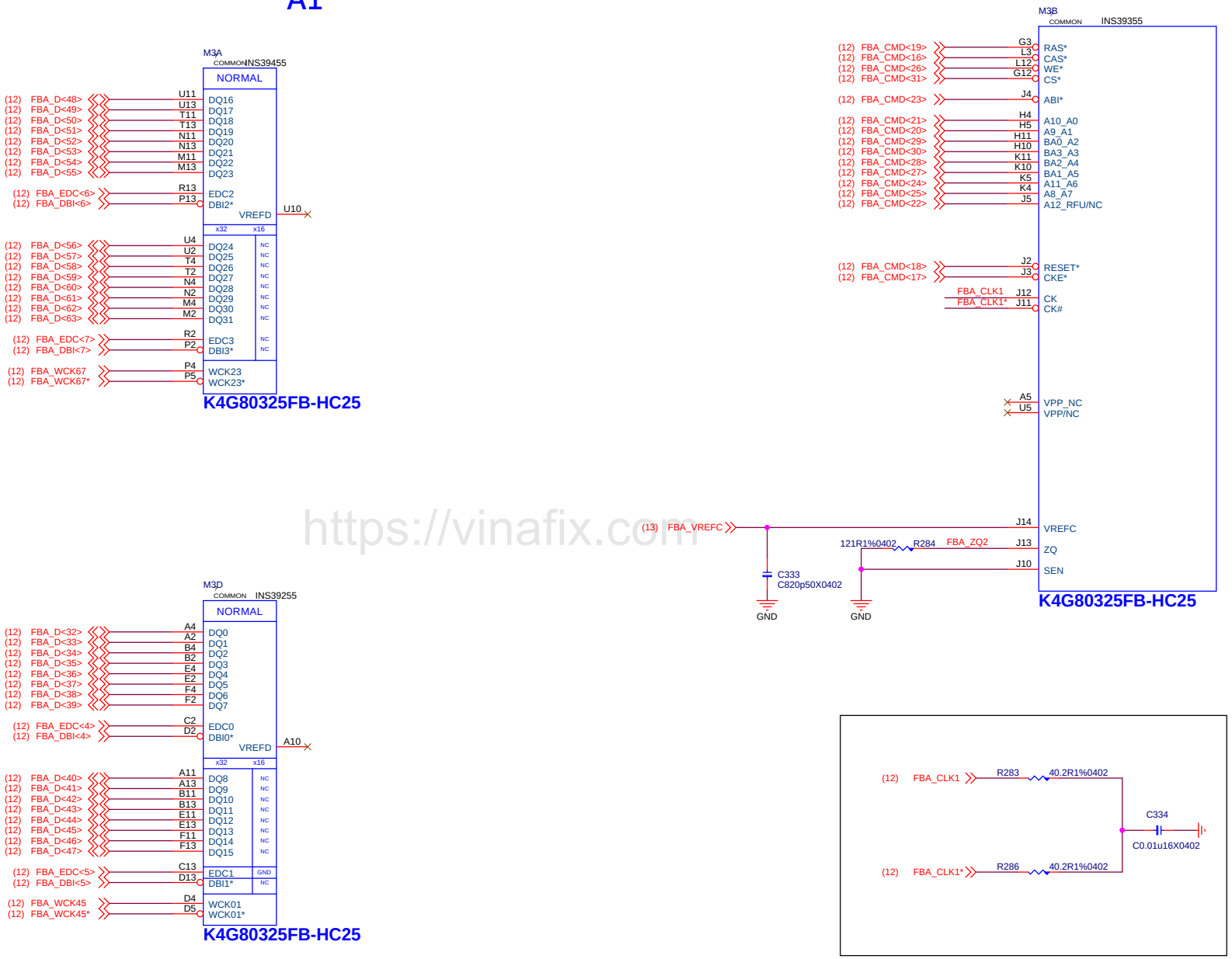
# DGPU_GDDR5 FrameBuffer
# A1

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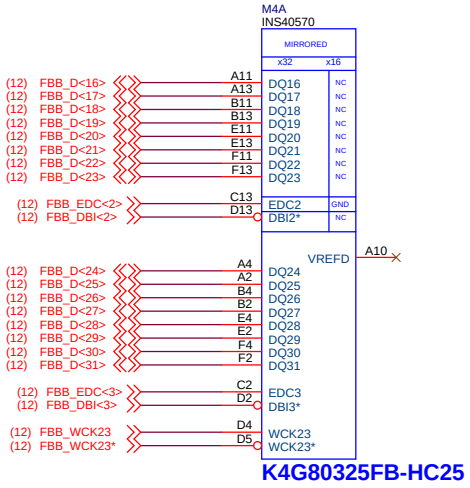
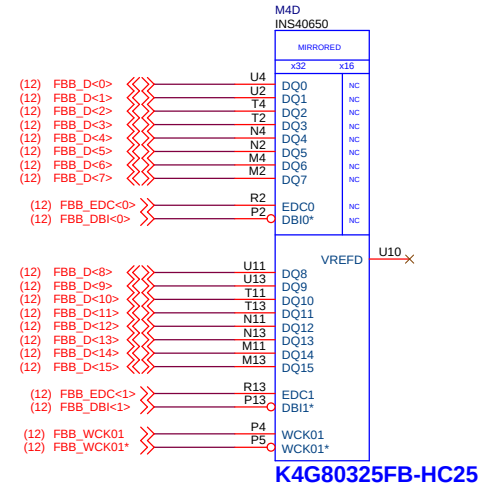
| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | |
| Title: DGPU_GDDR5 FrameBuffer A1 | | |
| Size: A3 | Document Number: MS-16K51 | Rev: 0B |
| Date: Thursday, October 05, 2017 | Sheet 14 of 80 | |

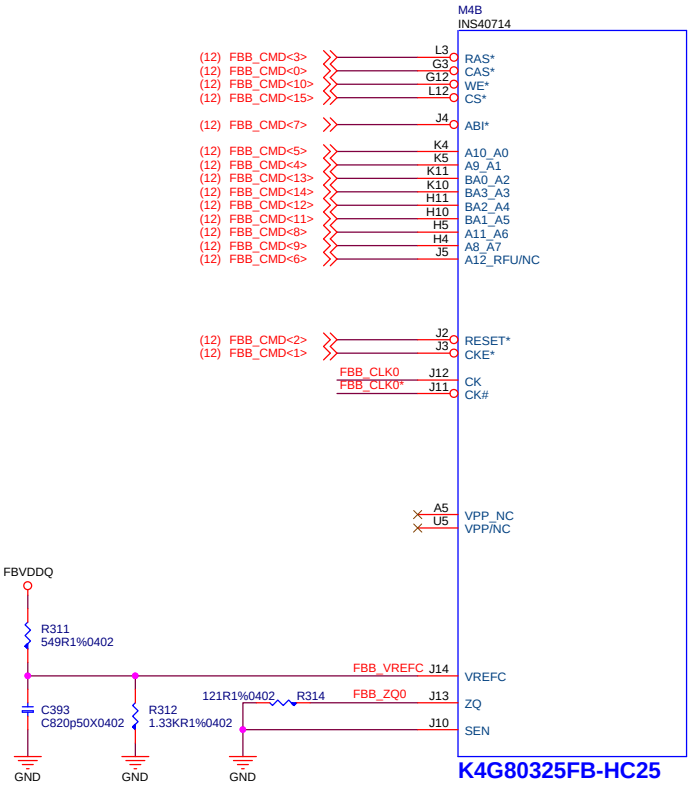
# DGPU_GDDR5 FrameBuffer B0



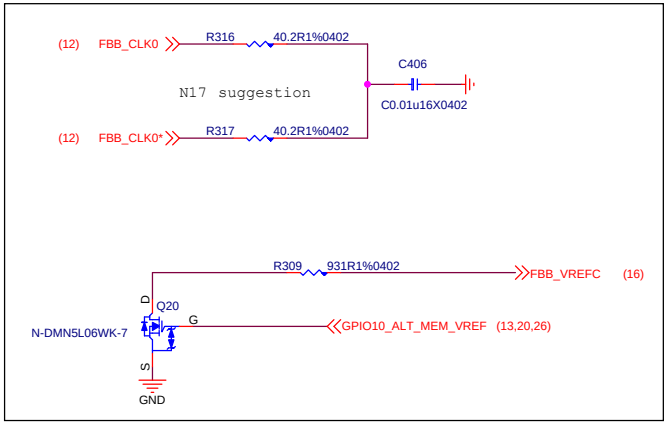

K4G80325FB-HC25




K4G80325FB-HC25




K4G80325FB-HC25

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Title: DGPU_GDDR5 FrameBuffer B0

Size: A3 | Document Number: MS-16K51 | Rev: 0B

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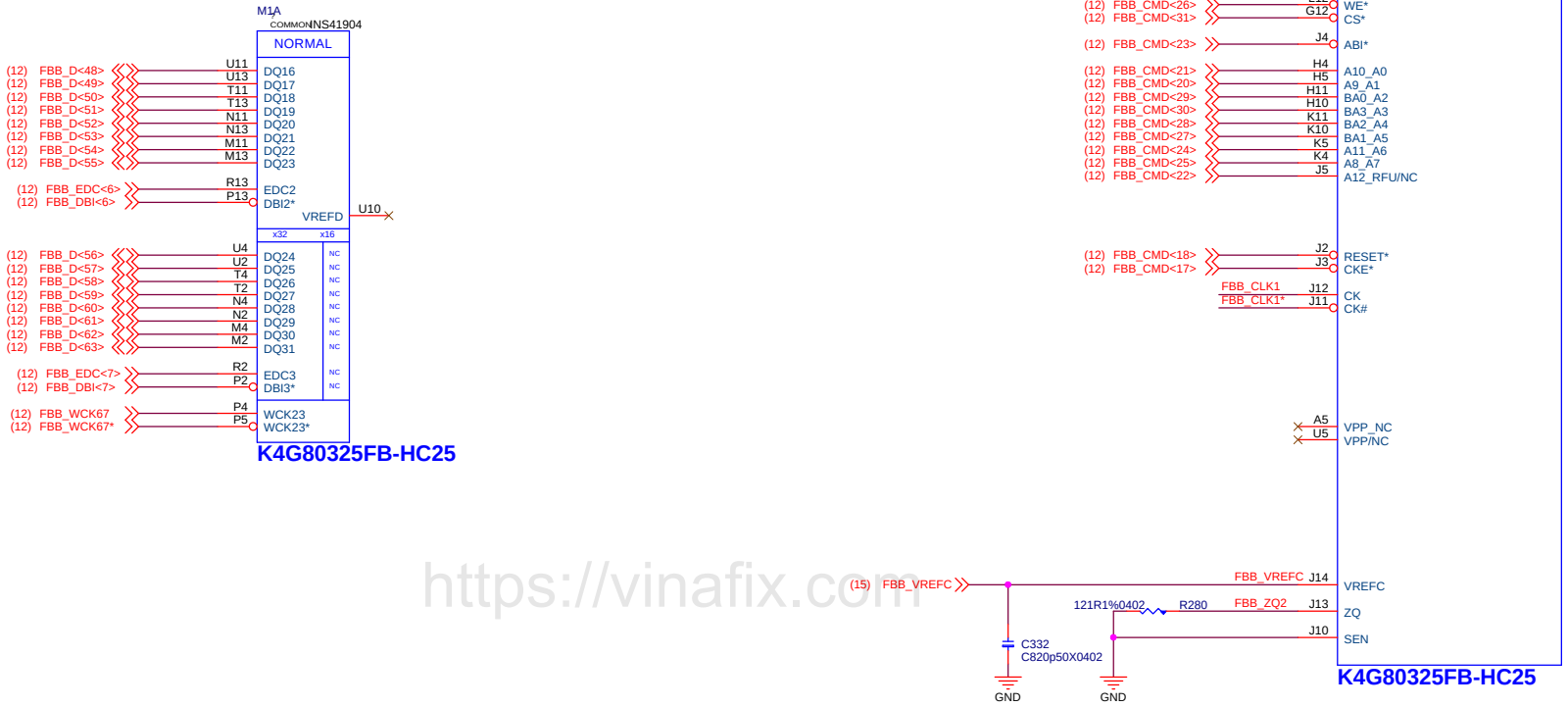
# DGPU_GDDR5 FrameBuffer B1

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| | | | |
|---|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | | |
| Title: DGPU_GDDR5 FrameBuffer B1 | | | |
| Size: A3 | Document Number: MS-16K51 | | Rev: 0B |
| Date: Thursday, October 05, 2017 | Sheet 16 of 80 | | |

# Frame Buffer Partition A Decoupling

FBVDDQ

SPARE

DECOUPLING AROUND FBA MEMORIES (DQ0-DQ31)

C300 C1u6.3X60402-RH, C296 C1u6.3X60402-RH, C324 C1u6.3X60402-RH, C18 C1u6.3X60402-RH, C345 C1u6.3X60402-RH, C348 C1u6.3X60402-RH, C16 C1u6.3X60402-RH, C13 C1u6.3X60402-RH, C313 C1u6.3X60402-RH, C346 C1u6.3X60402-RH, C321 C1u6.3X60402-RH, C356 C1u6.3X60402-RH, C315 C1u6.3X60402-RH, C352 C1u6.3X60402-RH, C339 C1u6.3X60402-RH, C6 C1u6.3X60402-RH, C349 C1u6.3X60402-RH, C327 C1u6.3X60402-RH

GND

4 X 10UF, 8 X 1UF X6S **Under Vram**

C15 C10u4X60603, C292 C10u4X60603, C9 C10u4X60603, C308 C10u4X60603

C307 C10u4X60603, C341 C10u4X60603

2 X 10UF, 5 X 22UF X6S

**Near Vram**

C1 C22u4X60603, C337 C22u4X60603, C11 C22u4X60603, C362 C22u4X60603, C2 C22u4X60603

M2C INS44015 — Mirrored

M3C COMMON INS44587 — Normal

| J1 | MF (add 1k to VDD) | | J1 | MF (add 1k to VSS) | |
|---|---|---|---|---|---|
| C10 | VDD_1 | VSS_1 B10 | B10 | VSS-1 | VDD-1 C10 |
| C5 | VDD_2 | VSS_2 B5 | B5 | VSS-2 | VDD-2 C5 |
| D11 | VDD_3 | VSS_3 D10 | D10 | VSS-3 | VDD-3 D11 |
| G1 | VDD_4 | VSS_4 G10 | G10 | VSS-4 | VDD-4 G1 |
| G11 | VDD_5 | VSS_5 G5 | G5 | VSS-5 | VDD-5 G11 |
| G14 | VDD_6 | VSS_6 H1 | H1 | VSS-6 | VDD-6 G14 |
| G4 | VDD_7 | VSS_7 H14 | H14 | VSS-7 | VDD-7 G4 |
| L1 | VDD_8 | VSS_8 K1 | K1 | VSS-8 | VDD-8 L1 |
| L11 | VDD_9 | VSS_9 K14 | K14 | VSS-9 | VDD-9 L11 |
| L14 | VDD_10 | VSS_10 L10 | L10 | VSS-10 | VDD-10 L14 |
| L4 | VDD_11 | VSS_11 L5 | L5 | VSS-11 | VDD-11 L4 |
| P11 | VDD_12 | VSS_12 P10 | P10 | VSS-12 | VDD-12 P11 |
| R10 | VDD_13 | VSS_13 T10 | T10 | VSS-13 | VDD-13 R10 |
| R5 | VDD_14 | VSS_14 T5 | T5 | VSS-14 | VDD-14 R5 |
| B1 | VDDQ_1 | VSSQ_1 A1 | A1 | VSSQ-1 | VDDQ-1 B1 |
| B12 | VDDQ_2 | VSSQ_2 A12 | A12 | VSSQ-2 | VDDQ-2 B12 |
| B14 | VDDQ_3 | VSSQ_3 A14 | A14 | VSSQ-3 | VDDQ-3 B14 |
| B3 | VDDQ_4 | VSSQ_4 A3 | A3 | VSSQ-4 | VDDQ-4 B3 |
| D1 | VDDQ_5 | VSSQ_5 C1 | C1 | VSSQ-5 | VDDQ-5 D1 |
| D12 | VDDQ_6 | VSSQ_6 C11 | C11 | VSSQ-6 | VDDQ-6 D12 |
| D14 | VDDQ_7 | VSSQ_7 C12 | C12 | VSSQ-7 | VDDQ-7 D14 |
| D3 | VDDQ_8 | VSSQ_8 C14 | C14 | VSSQ-8 | VDDQ-8 D3 |
| E10 | VDDQ_9 | VSSQ_9 C3 | C3 | VSSQ-9 | VDDQ-9 E10 |
| E5 | VDDQ_10 | VSSQ_10 C4 | C4 | VSSQ-10 | VDDQ-10 E5 |
| F1 | VDDQ_11 | VSSQ_11 E1 | E1 | VSSQ-11 | VDDQ-11 F1 |
| F12 | VDDQ_12 | VSSQ_12 E12 | E12 | VSSQ-12 | VDDQ-12 F12 |
| F14 | VDDQ_13 | VSSQ_13 E14 | E14 | VSSQ-13 | VDDQ-13 F14 |
| F3 | VDDQ_14 | VSSQ_14 E3 | E3 | VSSQ-14 | VDDQ-14 F3 |
| G13 | VDDQ_15 | VSSQ_15 F10 | F10 | VSSQ-15 | VDDQ-15 G13 |
| G2 | VDDQ_16 | VSSQ_16 F5 | F5 | VSSQ-16 | VDDQ-16 G2 |
| H12 | VDDQ_17 | VSSQ_17 H13 | H13 | VSSQ-17 | VDDQ-17 H12 |
| H3 | VDDQ_18 | VSSQ_18 H2 | H2 | VSSQ-18 | VDDQ-18 H3 |
| K12 | VDDQ_19 | VSSQ_19 K13 | K13 | VSSQ-19 | VDDQ-19 K12 |
| K3 | VDDQ_20 | VSSQ_20 K2 | K2 | VSSQ-20 | VDDQ-20 K3 |
| L13 | VDDQ_21 | VSSQ_21 M10 | M10 | VSSQ-21 | VDDQ-21 L13 |
| L2 | VDDQ_22 | VSSQ_22 M5 | M5 | VSSQ-22 | VDDQ-22 L2 |
| M1 | VDDQ_23 | VSSQ_23 N1 | N1 | VSSQ-23 | VDDQ-23 M1 |
| M12 | VDDQ_24 | VSSQ_24 N12 | N12 | VSSQ-24 | VDDQ-24 M12 |
| M14 | VDDQ_25 | VSSQ_25 N14 | N14 | VSSQ-25 | VDDQ-25 M14 |
| M3 | VDDQ_26 | VSSQ_26 N3 | N3 | VSSQ-26 | VDDQ-26 M3 |
| N10 | VDDQ_27 | VSSQ_27 R1 | R1 | VSSQ-27 | VDDQ-27 N10 |
| N5 | VDDQ_28 | VSSQ_28 R11 | R11 | VSSQ-28 | VDDQ-28 N5 |
| P1 | VDDQ_29 | VSSQ_29 R12 | R12 | VSSQ-29 | VDDQ-29 P1 |
| P12 | VDDQ_30 | VSSQ_30 R14 | R14 | VSSQ-30 | VDDQ-30 P12 |
| P14 | VDDQ_31 | VSSQ_31 R3 | R3 | VSSQ-31 | VDDQ-31 P14 |
| P3 | VDDQ_32 | VSSQ_32 R4 | R4 | VSSQ-32 | VDDQ-32 P3 |
| T1 | VDDQ_33 | VSSQ_33 U1 | U1 | VSSQ-33 | VDDQ-33 T1 |
| T12 | VDDQ_34 | VSSQ_34 U12 | U12 | VSSQ-34 | VDDQ-34 T12 |
| T14 | VDDQ_35 | VSSQ_35 U14 | U14 | VSSQ-35 | VDDQ-35 T14 |
| T3 | VDDQ_36 | VSSQ_36 U3 | U3 | VSSQ-36 | VDDQ-36 T3 |

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K4G80325FB-HC25

C294 C10u4X60603, C12 C10u4X60603, C319 C10u4X60603, C298 C10u4X60603

C293 C10u4X60603, C4 C10u4X60603

C291 C22u4X60603, C10 C22u4X60603, C5 C22u4X60603, C299 C22u4X60603, C3 C22u4X60603

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FBVDDQ

SPARE

DECOUPLING AROUND FBA MEMORIES (DQ32-DQ63)

C599 C1u6.3X60402-RH, C366 C1u6.3X60402-RH, C314 C1u6.3X60402-RH, C347 C1u6.3X60402-RH, C357 C1u6.3X60402-RH, C359 C1u6.3X60402-RH, C322 C1u6.3X60402-RH, C364 C1u6.3X60402-RH, C367 C1u6.3X60402-RH, C350 C1u6.3X60402-RH, C295 C1u6.3X60402-RH, C311 C1u6.3X60402-RH, C353 C1u6.3X60402-RH, C365 C1u6.3X60402-RH, C306 C1u6.3X60402-RH, C331 C1u6.3X60402-RH, C633 C1u6.3X60402-RH, C702 C1u6.3X60402-RH

GND

MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FB-A_DECOUPLING

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# Frame Buffer Partition B Decoupling

FBVDDQ

SPARE DECOUPLING AROUND FBB MEMORIES (DQ0-DQ31)

C425 C1u6.3X60402-RH, C398 C1u6.3X60402-RH, C19 C1u6.3X60402-RH, C438 C1u6.3X60402-RH, C363 C1u6.3X60402-RH, C323 C1u6.3X60402-RH, C442 C1u6.3X60402-RH, C351 C1u6.3X60402-RH, C317 C1u6.3X60402-RH, C409 C1u6.3X60402-RH, C453 C1u6.3X60402-RH, C495 C1u6.3X60402-RH, C408 C1u6.3X60402-RH, C396 C1u6.3X60402-RH, C397 C1u6.3X60402-RH, C402 C1u6.3X60402-RH, C318 C1u6.3X60402-RH, C312 C1u6.3X60402-RH

GND

FBVDDQ

C37 C10u4X60603, C432 C10u4X60603, C371 C10u4X60603, C410 C10u4X60603

GND

C39 C10u4X60603, C38 C10u4X60603

GND

C355 C22u4X60603, C756 C22u4X60603, C510 C22u4X60603, C742 C22u4X60603, C433 C22u4X60603

GND

FBVDDQ

M4C
INS47523
Mirrored

J1
MF
add 1k to VDD

| | | | |
|---|---|---|---|
| C10 | VDD_1 | VSS_1 | B10 |
| C5 | VDD_2 | VSS_2 | B5 |
| D11 | VDD_3 | VSS_3 | D10 |
| G1 | VDD_4 | VSS_4 | G10 |
| G11 | VDD_5 | VSS_5 | G5 |
| G14 | VDD_6 | VSS_6 | H1 |
| G4 | VDD_7 | VSS_7 | H14 |
| L1 | VDD_8 | VSS_8 | K1 |
| L11 | VDD_9 | VSS_9 | K14 |
| L14 | VDD_10 | VSS_10 | L10 |
| L4 | VDD_11 | VSS_11 | L5 |
| P11 | VDD_12 | VSS_12 | P10 |
| R10 | VDD_13 | VSS_13 | T10 |
| R5 | VDD_14 | VSS_14 | T5 |
| B1 | VDDQ_1 | VSSQ_1 | A1 |
| B12 | VDDQ_2 | VSSQ_2 | A12 |
| B14 | VDDQ_3 | VSSQ_3 | A14 |
| B3 | VDDQ_4 | VSSQ_4 | A3 |
| D1 | VDDQ_5 | VSSQ_5 | C1 |
| D12 | VDDQ_6 | VSSQ_6 | C11 |
| D14 | VDDQ_7 | VSSQ_7 | C12 |
| D3 | VDDQ_8 | VSSQ_8 | C14 |
| E10 | VDDQ_9 | VSSQ_9 | C3 |
| E5 | VDDQ_10 | VSSQ_10 | C4 |
| F1 | VDDQ_11 | VSSQ_11 | E1 |
| F12 | VDDQ_12 | VSSQ_12 | E12 |
| F14 | VDDQ_13 | VSSQ_13 | E14 |
| F3 | VDDQ_14 | VSSQ_14 | E3 |
| G13 | VDDQ_15 | VSSQ_15 | F10 |
| G2 | VDDQ_16 | VSSQ_16 | F5 |
| H12 | VDDQ_17 | VSSQ_17 | H13 |
| H3 | VDDQ_18 | VSSQ_18 | H2 |
| K12 | VDDQ_19 | VSSQ_19 | K13 |
| K3 | VDDQ_20 | VSSQ_20 | K2 |
| L13 | VDDQ_21 | VSSQ_21 | M10 |
| L2 | VDDQ_22 | VSSQ_22 | M5 |
| M1 | VDDQ_23 | VSSQ_23 | N1 |
| M12 | VDDQ_24 | VSSQ_24 | N12 |
| M14 | VDDQ_25 | VSSQ_25 | N14 |
| M3 | VDDQ_26 | VSSQ_26 | N3 |
| N10 | VDDQ_27 | VSSQ_27 | R1 |
| N5 | VDDQ_28 | VSSQ_28 | R11 |
| P1 | VDDQ_29 | VSSQ_29 | R12 |
| P12 | VDDQ_30 | VSSQ_30 | R14 |
| P14 | VDDQ_31 | VSSQ_31 | R3 |
| P3 | VDDQ_32 | VSSQ_32 | R4 |
| T1 | VDDQ_33 | VSSQ_33 | U1 |
| T12 | VDDQ_34 | VSSQ_34 | U12 |
| T14 | VDDQ_35 | VSSQ_35 | U14 |
| T3 | VDDQ_36 | VSSQ_36 | U3 |

K4G80325FB-HC25

GND

M1C
COMMON
INS48319
Normal

J1
MF
add 1k to VSS

| | | | |
|---|---|---|---|
| B10 | VSS-1 | VDD-1 | C10 |
| B5 | VSS-2 | VDD-2 | C5 |
| D10 | VSS-3 | VDD-3 | D11 |
| G10 | VSS-4 | VDD-4 | G1 |
| G5 | VSS-5 | VDD-5 | G11 |
| H1 | VSS-6 | VDD-6 | G14 |
| H14 | VSS-7 | VDD-7 | G4 |
| K1 | VSS-8 | VDD-8 | L1 |
| K14 | VSS-9 | VDD-9 | L11 |
| L10 | VSS-10 | VDD-10 | L14 |
| L5 | VSS-11 | VDD-11 | L4 |
| P10 | VSS-12 | VDD-12 | P11 |
| T10 | VSS-13 | VDD-13 | R10 |
| T5 | VSS-14 | VDD-14 | R5 |
| A1 | VSSQ-1 | VDDQ-1 | B1 |
| A12 | VSSQ-2 | VDDQ-2 | B12 |
| A14 | VSSQ-3 | VDDQ-3 | B14 |
| A3 | VSSQ-4 | VDDQ-4 | B3 |
| C1 | VSSQ-5 | VDDQ-5 | D1 |
| C11 | VSSQ-6 | VDDQ-6 | D12 |
| C12 | VSSQ-7 | VDDQ-7 | D14 |
| C14 | VSSQ-8 | VDDQ-8 | D3 |
| C3 | VSSQ-9 | VDDQ-9 | E10 |
| C4 | VSSQ-10 | VDDQ-10 | E5 |
| E1 | VSSQ-11 | VDDQ-11 | F1 |
| E12 | VSSQ-12 | VDDQ-12 | F12 |
| E14 | VSSQ-13 | VDDQ-13 | F14 |
| E3 | VSSQ-14 | VDDQ-14 | F3 |
| F10 | VSSQ-15 | VDDQ-15 | G13 |
| F5 | VSSQ-16 | VDDQ-16 | G2 |
| H13 | VSSQ-17 | VDDQ-17 | H12 |
| H2 | VSSQ-18 | VDDQ-18 | H3 |
| K13 | VSSQ-19 | VDDQ-19 | K12 |
| K2 | VSSQ-20 | VDDQ-20 | K3 |
| M10 | VSSQ-21 | VDDQ-21 | L13 |
| M5 | VSSQ-22 | VDDQ-22 | L2 |
| N1 | VSSQ-23 | VDDQ-23 | M1 |
| N12 | VSSQ-24 | VDDQ-24 | M12 |
| N14 | VSSQ-25 | VDDQ-25 | M14 |
| N3 | VSSQ-26 | VDDQ-26 | M3 |
| R1 | VSSQ-27 | VDDQ-27 | N10 |
| R11 | VSSQ-28 | VDDQ-28 | N5 |
| R12 | VSSQ-29 | VDDQ-29 | P1 |
| R14 | VSSQ-30 | VDDQ-30 | P12 |
| R3 | VSSQ-31 | VDDQ-31 | P14 |
| R4 | VSSQ-32 | VDDQ-32 | P3 |
| U1 | VSSQ-33 | VDDQ-33 | T1 |
| U12 | VSSQ-34 | VDDQ-34 | T12 |
| U14 | VSSQ-35 | VDDQ-35 | T14 |
| U3 | VSSQ-36 | VDDQ-36 | T3 |

K4G80325FB-HC25

GND

FBVDDQ

C303 C10u4X60603, C740 C10u4X60603, C302 C10u4X60603, C731 C10u4X60603

GND

C503 C10u4X60603, C297 C10u4X60603

GND

C305 C22u4X60603, C8 C22u4X60603, C7 C22u4X60603, C304 C22u4X60603, C283 C22u4X60603

GND

http://vinafix.com

FBVDDQ

SPARE DECOUPLING AROUND FBB MEMORIES (DQ32-DQ63)

C344 C1u6.3X60402-RH, C484 C1u6.3X60402-RH, C413 C1u6.3X60402-RH, C401 C1u6.3X60402-RH, C358 C1u6.3X60402-RH, C328 C1u6.3X60402-RH, C407 C1u6.3X60402-RH, C316 C1u6.3X60402-RH, C325 C1u6.3X60402-RH, C621 C1u6.3X60402-RH, C338 C1u6.3X60402-RH, C309 C1u6.3X60402-RH, C343 C1u6.3X60402-RH, C326 C1u6.3X60402-RH, C320 C1u6.3X60402-RH, C637 C1u6.3X60402-RH, C354 C1u6.3X60402-RH, C329 C1u6.3X60402-RH

GND

MICRO-STAR INT'L CO.,LTD.

| | | |
|---|---|---|
| Title | DGPU_GDDR5 FB-B_DECOUPLING | |
| Size A3 | Document Number MS-16K51 | Rev 0B |
| Date: Thursday, October 05, 2017 | Sheet 18 of 80 | |

# GPU Frame Buffer Partition C/D

G1D
INS50251
BGA2152
COMMON

4/23 FBC

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| (20) FBC_D<0> | C6 | FBC_D0 | FBC_CMD0 | C11 | FBC_CMD<0> (20) | | |
| (20) FBC_D<1> | D6 | FBC_D1 | FBC_CMD1 | B11 | FBC_CMD<1> (20) | | |
| (20) FBC_D<2> | A6 | FBC_D2 | FBC_CMD2 | A11 | FBC_CMD<2> (20) | | |
| (20) FBC_D<3> | B6 | FBC_D3 | FBC_CMD3 | D11 | FBC_CMD<3> (20) | | |
| (20) FBC_D<4> | B4 | FBC_D4 | FBC_CMD4 | A12 | FBC_CMD<4> (20) | | |
| (20) FBC_D<5> | A4 | FBC_D5 | FBC_CMD5 | B12 | FBC_CMD<5> (20) | | |
| (20) FBC_D<6> | B3 | FBC_D6 | FBC_CMD6 | C12 | FBC_CMD<6> (20) | | |
| (20) FBC_D<7> | C4 | FBC_D7 | FBC_CMD7 | C14 | FBC_CMD<7> (20) | | |
| (20) FBC_D<8> | D9 | FBC_D8 | FBC_CMD8 | B14 | FBC_CMD<8> (20) | | |
| (20) FBC_D<9> | C9 | FBC_D9 | FBC_CMD9 | A14 | FBC_CMD<9> (20) | | |
| (20) FBC_D<10> | E9 | FBC_D10 | FBC_CMD10 | D14 | FBC_CMD<10> (20) | | |
| (20) FBC_D<11> | B9 | FBC_D11 | FBC_CMD11 | A15 | FBC_CMD<11> (20) | | |
| (20) FBC_D<12> | B8 | FBC_D12 | FBC_CMD12 | B15 | FBC_CMD<12> (20) | | |
| (20) FBC_D<13> | A8 | FBC_D13 | FBC_CMD13 | C15 | FBC_CMD<13> (20) | | |
| (20) FBC_D<14> | F6 | FBC_D14 | FBC_CMD14 | C17 | FBC_CMD<14> (20) | | |
| (20) FBC_D<15> | E6 | FBC_D15 | FBC_CMD15 | B17 | FBC_CMD<15> (20) | | |
| (20) FBC_D<16> | F18 | FBC_D16 | FBC_CMD16 | B24 | FBC_CMD<16> (21) | | |
| (20) FBC_D<17> | G18 | FBC_D17 | FBC_CMD17 | A24 | FBC_CMD<17> (21) | | |
| (20) FBC_D<18> | E18 | FBC_D18 | FBC_CMD18 | D23 | FBC_CMD<18> (21) | | |
| (20) FBC_D<19> | H18 | FBC_D19 | FBC_CMD19 | A23 | FBC_CMD<19> (21) | | |
| (20) FBC_D<20> | D15 | FBC_D20 | FBC_CMD20 | B23 | FBC_CMD<20> (21) | | |
| (20) FBC_D<21> | E15 | FBC_D21 | FBC_CMD21 | C23 | FBC_CMD<21> (21) | | |
| (20) FBC_D<22> | G17 | FBC_D22 | FBC_CMD22 | C21 | FBC_CMD<22> (21) | | |
| (20) FBC_D<23> | H17 | FBC_D23 | FBC_CMD23 | B21 | FBC_CMD<23> (21) | | |
| (20) FBC_D<24> | J15 | FBC_D24 | FBC_CMD24 | A21 | FBC_CMD<24> (21) | | |
| (20) FBC_D<25> | H15 | FBC_D25 | FBC_CMD25 | D20 | FBC_CMD<25> (21) | | |
| (20) FBC_D<26> | E14 | FBC_D26 | FBC_CMD26 | A20 | FBC_CMD<26> (21) | | |
| (20) FBC_D<27> | F14 | FBC_D27 | FBC_CMD27 | B20 | FBC_CMD<27> (21) | | |
| (20) FBC_D<28> | H11 | FBC_D28 | FBC_CMD28 | C20 | FBC_CMD<28> (21) | | |
| (20) FBC_D<29> | G11 | FBC_D29 | FBC_CMD29 | C18 | FBC_CMD<29> (21) | | |
| (20) FBC_D<30> | F11 | FBC_D30 | FBC_CMD30 | B18 | FBC_CMD<30> (21) | | |
| (20) FBC_D<31> | E11 | FBC_D31 | FBC_CMD31 | A18 | FBC_CMD<31> (21) | | |
| (21) FBC_D<32> | J29 | FBC_D32 | FBC_CMD32 | D17 | | | |
| (21) FBC_D<33> | F30 | FBC_D33 | FBC_CMD33 | A17 | | | |
| (21) FBC_D<34> | H29 | FBC_D34 | FBC_CMD34 | A9 | | | |
| (21) FBC_D<35> | G30 | FBC_D35 | FBC_CMD35 | C24 | | | |
| (21) FBC_D<36> | B30 | FBC_D36 | | | | | |
| (21) FBC_D<37> | A30 | FBC_D37 | FBC_DBG_RFU1 | J14 | | | |
| (21) FBC_D<38> | H30 | FBC_D38 | FBC_DBG_RFU2 | J23 | | | |
| (21) FBC_D<39> | C30 | FBC_D39 | | | | | |
| (21) FBC_D<40> | D27 | FBC_D40 | FBC_CLK0 | G15 | FBC_CLK0 (20) | | |
| (21) FBC_D<41> | J26 | FBC_D41 | FBC_CLK0 | F15 | FBC_CLK0* (20) | | |
| (21) FBC_D<42> | F27 | FBC_D42 | FBC_CLK1 | H21 | FBC_CLK1 (21) | | |
| (21) FBC_D<43> | G27 | FBC_D43 | FBC_CLK1 | J21 | FBC_CLK1* (21) | | |
| (21) FBC_D<44> | C27 | FBC_D44 | | | | | |
| (21) FBC_D<45> | B27 | FBC_D45 | | | | | |
| (21) FBC_D<46> | A27 | FBC_D46 | | | | | |
| (21) FBC_D<47> | G29 | FBC_D47 | | | | | |
| (21) FBC_D<48> | H20 | FBC_D48 | | | | | |
| (21) FBC_D<49> | D18 | FBC_D49 | | | | | |
| (21) FBC_D<50> | G20 | FBC_D50 | | | | | |
| (21) FBC_D<51> | E20 | FBC_D51 | | | | | |
| (21) FBC_D<52> | F23 | FBC_D52 | | | | | |
| (21) FBC_D<53> | E21 | FBC_D53 | | | | | |
| (21) FBC_D<54> | D21 | FBC_D54 | | | | | |
| (21) FBC_D<55> | E23 | FBC_D55 | | | | | |
| (21) FBC_D<56> | G24 | FBC_D56 | FBC_WCK01 | F8 | FBC_WCK01 (20) | | |
| (21) FBC_D<57> | H26 | FBC_D57 | FBC_WCK01 | G8 | FBC_WCK01* (20) | | |
| (21) FBC_D<58> | F24 | FBC_D58 | FBC_WCKB01 | G9 | | | |
| (21) FBC_D<59> | G26 | FBC_D59 | FBC_WCKB01 | F9 | | | |
| (21) FBC_D<60> | F26 | FBC_D60 | FBC_WCK23 | H12 | FBC_WCK23 (20) | | |
| (21) FBC_D<61> | D26 | FBC_D61 | FBC_WCK23 | G12 | FBC_WCK23* (20) | | |
| (21) FBC_D<62> | B26 | FBC_D62 | FBC_WCKB23 | G14 | | | |
| (21) FBC_D<63> | C26 | FBC_D63 | FBC_WCKB23 | H14 | | | |
| | | | FBC_WCK45 | J27 | FBC_WCK45 (21) | | |
| | | | FBC_WCK45 | H27 | FBC_WCK45* (21) | | |
| (20) FBC_DBI<0> | A5 | FBC_DQM0 | FBC_WCKB45 | E29 | | | |
| (20) FBC_DBI<1> | C8 | FBC_DQM1 | FBC_WCKB45 | F29 | | | |
| (20) FBC_DBI<2> | J18 | FBC_DQM2 | FBC_WCK67 | G23 | FBC_WCK67 (21) | | |
| (20) FBC_DBI<3> | F12 | FBC_DQM3 | FBC_WCK67 | H23 | FBC_WCK67* (21) | | |
| (21) FBC_DBI<4> | D29 | FBC_DQM4 | FBC_WCKB67 | H24 | | | |
| (21) FBC_DBI<5> | E27 | FBC_DQM5 | FBC_WCKB67 | J24 | | | |
| (21) FBC_DBI<6> | F20 | FBC_DQM6 | | | | | |
| (21) FBC_DBI<7> | E26 | FBC_DQM7 | | | | | |
| (20) FBC_EDC<0> | D5 | FBC_DQS_WP0 | | | | | |
| (20) FBC_EDC<1> | D8 | FBC_DQS_WP1 | | | | | |
| (20) FBC_EDC<2> | E17 | FBC_DQS_WP2 | | | | | |
| (20) FBC_EDC<3> | E12 | FBC_DQS_WP3 | | | | | |
| (21) FBC_EDC<4> | E30 | FBC_DQS_WP4 | | | | | |
| (21) FBC_EDC<5> | B29 | FBC_DQS_WP5 | | | | | |
| (21) FBC_EDC<6> | G21 | FBC_DQS_WP6 | | | | | |
| (21) FBC_EDC<7> | E24 | FBC_DQS_WP7 | | | | | |
| | Y25 | GND | | | | | |
| | Y26 | GND | | | | | |
| | Y27 | GND | | | | | |
| | Y28 | GND | | | | | |
| | Y29 | GND | | | | | |
| | Y30 | GND | | | | | |
| | Y31 | GND | | | | | |
| | Y32 | GND | | | | | |

GND

FBC_PLL_AVDD L17 — PLACE AT BALLS — FB_PLLAVDD (12)

C689 C0.1u50X0402-HF

GND

**0.1uF*1 X7R**

FBVDDQ

R363 10KR1%0402 — R335 10KR1%0402

FBC_CMD<1>
FBC_CMD<17>

FBC_CMD<2>
FBC_CMD<18>

R334 10KR1%0402 — R366 10KR1%0402

GND

GDDR5 Mapping By GB4-256

| | 0..31 | 32..63 |
|---|---|---|
| CMD0 | CAS* | |
| CMD1 | CKE* | |
| CMD2 | RST* | |
| CMD3 | RAS* | |
| CMD4 | A1_A9 | |
| CMD5 | A0_A10 | |
| CMD6 | A12_RFU | |
| CMD7 | ABI* | |
| CMD8 | A6_A11 | |
| CMD9 | A7_A8 | |
| CMD10 | WE* | |
| CMD11 | A5_BA1 | |
| CMD12 | A4_BA2 | |
| CMD13 | A2_BA0 | |
| CMD14 | A3_BA3 | |
| CMD15 | CS* | |
| CMD16 | | CAS* |
| CMD17 | | CKE* |
| CMD18 | | RST* |
| CMD19 | | RAS* |
| CMD20 | | A1_A9 |
| CMD21 | | A0_A10 |
| CMD22 | | A12_RFU |
| CMD23 | | ABI* |
| CMD24 | | A6_A11 |
| CMD25 | | A7_A8 |
| CMD26 | | WE* |
| CMD27 | | A5_BA1 |
| CMD28 | | A4_BA2 |
| CMD29 | | A2_BA0 |
| CMD30 | | A3_BA3 |
| CMD31 | | CS* |

https://manx.com

G1E
INS51185
BGA2152
COMMON

5/23 FBD

| | | | | | |
|---|---|---|---|---|---|
| AK8 | FBD_D0 | FBD_CMD0 | AD2 | | |
| AK4 | FBD_D1 | FBD_CMD1 | AD1 | | |
| AK2 | FBD_D2 | FBD_CMD2 | AD4 | | |
| AK3 | FBD_D3 | FBD_CMD3 | AC1 | | |
| AK5 | FBD_D4 | FBD_CMD4 | AC2 | | |
| AK6 | FBD_D5 | FBD_CMD5 | AC3 | | |
| AK9 | FBD_D6 | FBD_CMD6 | AA3 | | |
| AK7 | FBD_D7 | FBD_CMD7 | AA2 | | |
| AG4 | FBD_D8 | FBD_CMD8 | AA1 | | |
| AF9 | FBD_D9 | FBD_CMD9 | AA4 | | |
| AG6 | FBD_D10 | FBD_CMD10 | Y1 | | |
| AG7 | FBD_D11 | FBD_CMD11 | Y2 | | |
| AJ4 | FBD_D12 | FBD_CMD12 | Y3 | | |
| AJ5 | FBD_D13 | FBD_CMD13 | V3 | | |
| AJ6 | FBD_D14 | FBD_CMD14 | V2 | | |
| AG5 | FBD_D15 | FBD_CMD15 | V1 | | |
| Y6 | FBD_D16 | FBD_CMD16 | L3 | | |
| Y5 | FBD_D17 | FBD_CMD17 | L2 | | |
| V5 | FBD_D18 | FBD_CMD18 | L1 | | |
| Y4 | FBD_D19 | FBD_CMD19 | M4 | | |
| AA6 | FBD_D20 | FBD_CMD20 | M1 | | |
| AA5 | FBD_D21 | FBD_CMD21 | M2 | | |
| AC5 | FBD_D22 | FBD_CMD22 | M3 | | |
| AC4 | FBD_D23 | FBD_CMD23 | P3 | | |
| AD7 | FBD_D24 | FBD_CMD24 | P2 | | |
| AC6 | FBD_D25 | FBD_CMD25 | P1 | | |
| AF6 | FBD_D26 | FBD_CMD26 | R4 | | |
| AD6 | FBD_D27 | FBD_CMD27 | R1 | | |
| AF7 | FBD_D28 | FBD_CMD28 | R2 | | |
| AF8 | FBD_D29 | FBD_CMD29 | R3 | | |
| AF2 | FBD_D30 | FBD_CMD30 | U3 | | |
| AF3 | FBD_D31 | FBD_CMD31 | U2 | | |
| F4 | FBD_D32 | FBD_CMD32 | U1 | | |
| E1 | FBD_D33 | FBD_CMD33 | V4 | | |
| F3 | FBD_D34 | FBD_CMD34 | AD3 | | |
| F5 | FBD_D35 | FBD_CMD35 | J3 | | |
| D2 | FBD_D36 | | | | |
| D1 | FBD_D37 | FBD_DBG_RFU1 | AC9 | | |
| C3 | FBD_D38 | FBD_DBG_RFU2 | P9 | | |
| C2 | FBD_D39 | | | | |
| J5 | FBD_D40 | FBD_CLK0 | Y8 | | |
| J4 | FBD_D41 | FBD_CLK0 | Y7 | | |
| L3 | FBD_D42 | FBD_CLK1 | R8 | | |
| J2 | FBD_D43 | FBD_CLK1 | R7 | | |
| F1 | FBD_D44 | | | | |
| F2 | FBD_D45 | | | | |
| H4 | FBD_D46 | | | | |
| H5 | FBD_D47 | | | | |
| V7 | FBD_D48 | | | | |
| V8 | FBD_D49 | | | | |
| V6 | FBD_D50 | | | | |
| V9 | FBD_D51 | | | | |
| U4 | FBD_D52 | | | | |
| R5 | FBD_D53 | | | | |
| R6 | FBD_D54 | | | | |
| U8 | FBD_D55 | | | | |
| P8 | FBD_D56 | FBD_WCK01 | AJ8 | | |
| R9 | FBD_D57 | FBD_WCK01 | AJ7 | | |
| P4 | FBD_D58 | FBD_WCKB01 | AG8 | | |
| P5 | FBD_D59 | FBD_WCKB01 | AG9 | | |
| L7 | FBD_D60 | FBD_WCK23 | AD8 | | |
| L6 | FBD_D61 | FBD_WCK23 | AD9 | | |
| L4 | FBD_D62 | FBD_WCKB23 | AC7 | | |
| L5 | FBD_D63 | FBD_WCKB23 | AC8 | | |
| | | FBD_WCK45 | J6 | | |
| | | FBD_WCK45 | J7 | | |
| AJ1 | FBD_DQM0 | FBD_WCKB45 | H7 | | |
| AG1 | FBD_DQM1 | FBD_WCKB45 | H6 | | |
| AA2 | FBD_DQM2 | FBD_WCK67 | P8 | | |
| AD5 | FBD_DQM3 | FBD_WCK67 | P7 | | |
| D3 | FBD_DQM4 | FBD_WCKB67 | M7 | | |
| H3 | FBD_DQM5 | FBD_WCKB67 | M8 | | |
| U5 | FBD_DQM6 | | | | |
| M9 | FBD_DQM7 | | | | |
| AJ3 | FBD_DQS_WP0 | | | | |
| AG2 | FBD_DQS_WP1 | | | | |
| AA9 | FBD_DQS_WP2 | | | | |
| AF4 | FBD_DQS_WP3 | | | | |
| E3 | FBD_DQS_WP4 | | | | |
| H2 | FBD_DQS_WP5 | | | | |
| U6 | FBD_DQS_WP6 | | | | |
| M5 | FBD_DQS_WP7 | | | | |
| Y33 | GND | | | | |
| Y34 | GND | | | | |
| Y35 | GND | | | | |
| Y36 | GND | | | | |
| Y37 | GND | | | | |
| Y38 | GND | | | | |
| Y39 | GND | | | | |
| Y9 | GND | | | | |

GND

FBD_PLL_AVDD V11 — PLACE AT BALLS — FB_PLLAVDD

C472 C0.1u50X0402-HF

GND

**0.1uF*1 X7R**

| GP104 | GP106 |
|---|---|
| FBD | UNUSED |

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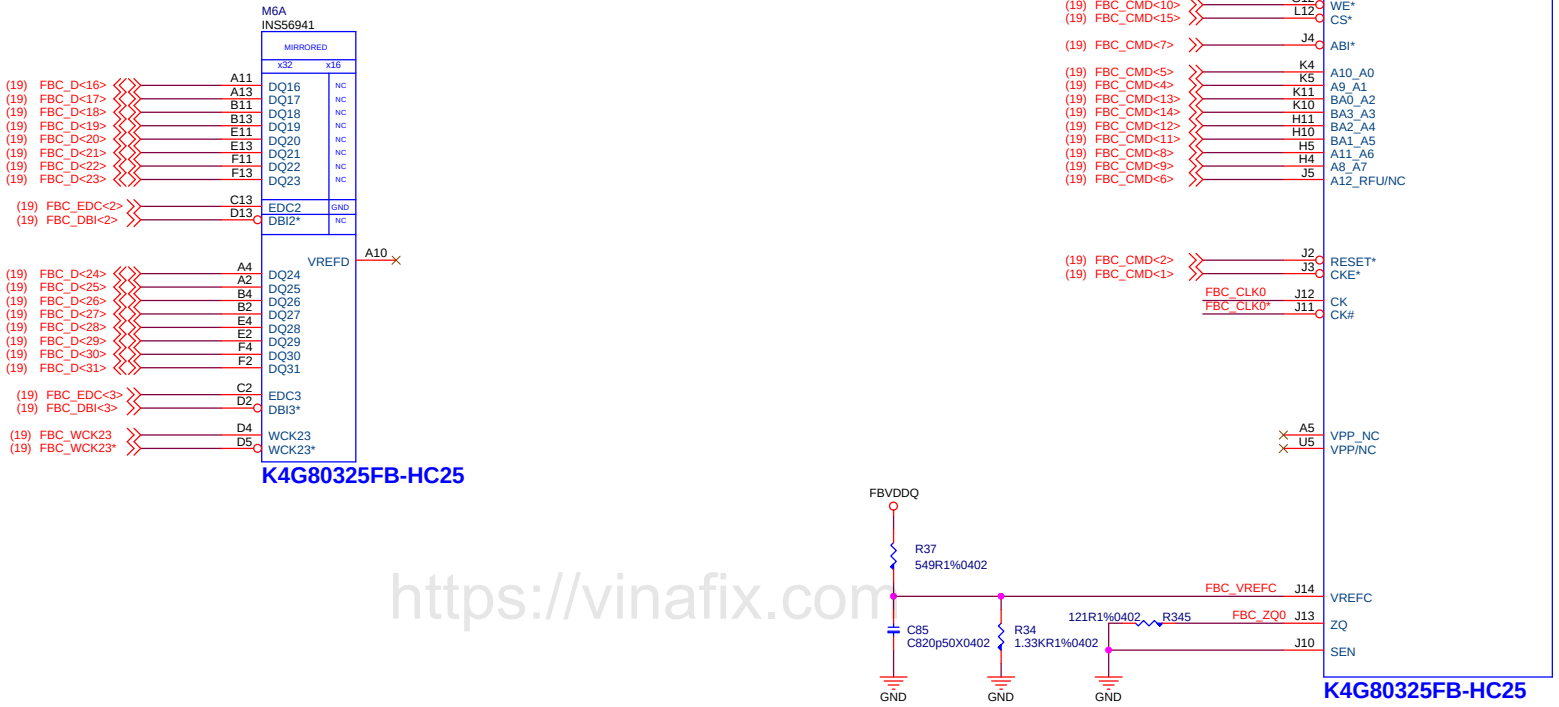
Title: DGPU_MEM IF C/D

Size: Custom | Document Number: MS-16K51 | Rev: 0B

Date: Thursday, October 05, 2017 | Sheet 19 of 80

# DGPU_GDDR5 FrameBuffer
# C0

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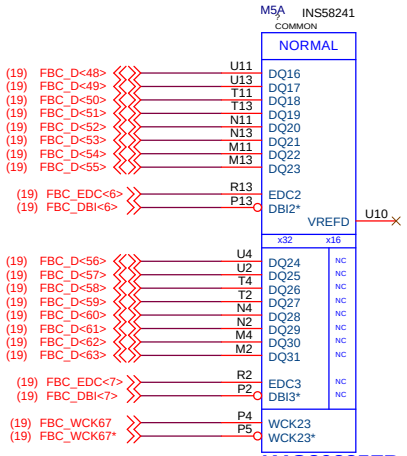
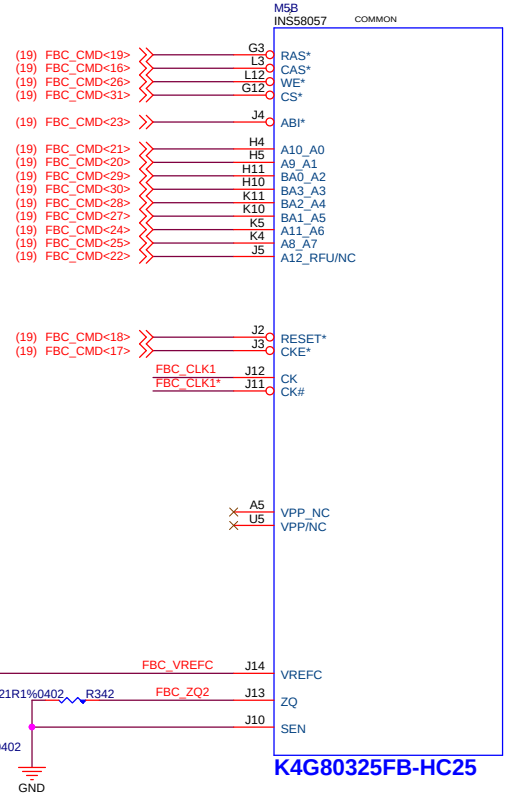
Title: DGPU_GDDR5 FrameBuffer C

Size: A3 | Document Number: MS-16K51 | Rev: 0B

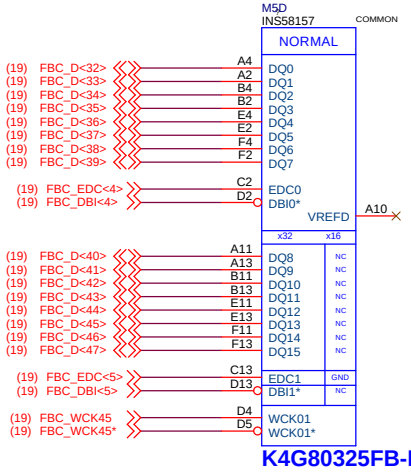
Date: Thursday, October 05, 2017 | Sheet 20 of 80

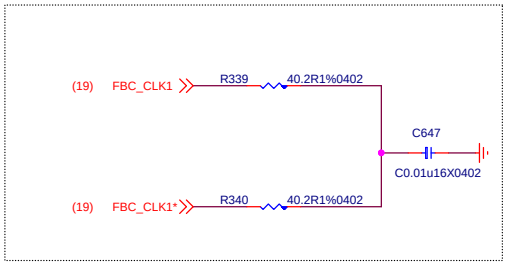
# DGPU_GDDR5 FrameBuffer
# C1




https://vinafix.com




MICRO-STAR INT'L CO.,LTD.

Title: DGPU_GDDR5 FrameBuffer C

Size: A3 | Document Number: MS-16K51 | Rev: 0B

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# Frame Buffer Partition C Decoupling

SPARE DECOUPLING AROUND FBC MEMORIES (DQ0-DQ31)

FBVDDQ

C103 C1u6.3X60402-RH, C536 C1u6.3X60402-RH, C535 C1u6.3X60402-RH, C537 C1u6.3X60402-RH, C659 C1u6.3X60402-RH, C68 C1u6.3X60402-RH, C67 C1u6.3X60402-RH, C92 C1u6.3X60402-RH, C746 C1u6.3X60402-RH, C655 C1u6.3X60402-RH, C754 C1u6.3X60402-RH, C667 C1u6.3X60402-RH, C747 C1u6.3X60402-RH, C692 C1u6.3X60402-RH, C677 C1u6.3X60402-RH, C654 C1u6.3X60402-RH, C645 C1u6.3X60402-RH, C675 C1u6.3X60402-RH

GND

FBVDDQ

C737 C10u4X60603, C389 C10u4X60603, C99 C10u4X60603, C760 C10u4X60603

GND

C757 C10u4X60603, C719 C10u4X60603

GND

C635 C22u4X60603, C100 C22u4X60603, C89 C22u4X60603, C712 C22u4X60603, C761 C22u4X60603

GND

FBVDDQ

M6C
INS61344
Mirrored

J1
MF add 1k to VDD

| | | | |
|---|---|---|---|
| C10 | VDD_1 | VSS_1 | B10 |
| C5 | VDD_2 | VSS_2 | B5 |
| D11 | VDD_3 | VSS_3 | D10 |
| G1 | VDD_4 | VSS_4 | G10 |
| G11 | VDD_5 | VSS_5 | G5 |
| G14 | VDD_6 | VSS_6 | H1 |
| G4 | VDD_7 | VSS_7 | H14 |
| L1 | VDD_8 | VSS_8 | K1 |
| L11 | VDD_9 | VSS_9 | K14 |
| L14 | VDD_10 | VSS_10 | L10 |
| L4 | VDD_11 | VSS_11 | L5 |
| P11 | VDD_12 | VSS_12 | P10 |
| R10 | VDD_13 | VSS_13 | T10 |
| R5 | VDD_14 | VSS_14 | T5 |
| B1 | VDDQ_1 | VSSQ_1 | A1 |
| B12 | VDDQ_2 | VSSQ_2 | A12 |
| B14 | VDDQ_3 | VSSQ_3 | A14 |
| B3 | VDDQ_4 | VSSQ_4 | A3 |
| D1 | VDDQ_5 | VSSQ_5 | C1 |
| D12 | VDDQ_6 | VSSQ_6 | C11 |
| D14 | VDDQ_7 | VSSQ_7 | C12 |
| D3 | VDDQ_8 | VSSQ_8 | C14 |
| E10 | VDDQ_9 | VSSQ_9 | C3 |
| E5 | VDDQ_10 | VSSQ_10 | C4 |
| F1 | VDDQ_11 | VSSQ_11 | E1 |
| F12 | VDDQ_12 | VSSQ_12 | E12 |
| F14 | VDDQ_13 | VSSQ_13 | E14 |
| F3 | VDDQ_14 | VSSQ_14 | E3 |
| G13 | VDDQ_15 | VSSQ_15 | F10 |
| G2 | VDDQ_16 | VSSQ_16 | F5 |
| H12 | VDDQ_17 | VSSQ_17 | H13 |
| H3 | VDDQ_18 | VSSQ_18 | H2 |
| K12 | VDDQ_19 | VSSQ_19 | K13 |
| K3 | VDDQ_20 | VSSQ_20 | K2 |
| L13 | VDDQ_21 | VSSQ_21 | M10 |
| L2 | VDDQ_22 | VSSQ_22 | M5 |
| M1 | VDDQ_23 | VSSQ_23 | N1 |
| M12 | VDDQ_24 | VSSQ_24 | N12 |
| M14 | VDDQ_25 | VSSQ_25 | N14 |
| M3 | VDDQ_26 | VSSQ_26 | N3 |
| N10 | VDDQ_27 | VSSQ_27 | R1 |
| N5 | VDDQ_28 | VSSQ_28 | R11 |
| P1 | VDDQ_29 | VSSQ_29 | R12 |
| P12 | VDDQ_30 | VSSQ_30 | R14 |
| P14 | VDDQ_31 | VSSQ_31 | R3 |
| P3 | VDDQ_32 | VSSQ_32 | R4 |
| T1 | VDDQ_33 | VSSQ_33 | U1 |
| T12 | VDDQ_34 | VSSQ_34 | U12 |
| T14 | VDDQ_35 | VSSQ_35 | U14 |
| T3 | VDDQ_36 | VSSQ_36 | U3 |

K4G80325FB-HC25

GND

M5C
INS60352
COMMON
Normal

J1
MF add 1k to VSS

| | | | |
|---|---|---|---|
| B10 | VSS-1 | VDD-1 | C10 |
| B5 | VSS-2 | VDD-2 | C5 |
| D10 | VSS-3 | VDD-3 | D11 |
| G10 | VSS-4 | VDD-4 | G1 |
| G5 | VSS-5 | VDD-5 | G11 |
| H1 | VSS-6 | VDD-6 | G14 |
| H14 | VSS-7 | VDD-7 | G4 |
| K1 | VSS-8 | VDD-8 | L1 |
| K14 | VSS-9 | VDD-9 | L11 |
| L10 | VSS-10 | VDD-10 | L14 |
| L5 | VSS-11 | VDD-11 | L4 |
| P10 | VSS-12 | VDD-12 | P11 |
| T10 | VSS-13 | VDD-13 | R10 |
| T5 | VSS-14 | VDD-14 | R5 |
| A1 | VSSQ-1 | VDDQ-1 | B1 |
| A12 | VSSQ-2 | VDDQ-2 | B12 |
| A14 | VSSQ-3 | VDDQ-3 | B14 |
| A3 | VSSQ-4 | VDDQ-4 | B3 |
| C1 | VSSQ-5 | VDDQ-5 | D1 |
| C11 | VSSQ-6 | VDDQ-6 | D12 |
| C12 | VSSQ-7 | VDDQ-7 | D14 |
| C14 | VSSQ-8 | VDDQ-8 | D3 |
| C3 | VSSQ-9 | VDDQ-9 | E10 |
| C4 | VSSQ-10 | VDDQ-10 | E5 |
| E1 | VSSQ-11 | VDDQ-11 | F1 |
| E12 | VSSQ-12 | VDDQ-12 | F12 |
| E14 | VSSQ-13 | VDDQ-13 | F14 |
| E3 | VSSQ-14 | VDDQ-14 | F3 |
| F10 | VSSQ-15 | VDDQ-15 | G13 |
| F5 | VSSQ-16 | VDDQ-16 | G2 |
| H13 | VSSQ-17 | VDDQ-17 | H12 |
| H2 | VSSQ-18 | VDDQ-18 | H3 |
| K13 | VSSQ-19 | VDDQ-19 | K12 |
| K2 | VSSQ-20 | VDDQ-20 | K3 |
| M10 | VSSQ-21 | VDDQ-21 | L13 |
| M5 | VSSQ-22 | VDDQ-22 | L2 |
| N1 | VSSQ-23 | VDDQ-23 | M1 |
| N12 | VSSQ-24 | VDDQ-24 | M12 |
| N14 | VSSQ-25 | VDDQ-25 | M14 |
| N3 | VSSQ-26 | VDDQ-26 | M3 |
| R1 | VSSQ-27 | VDDQ-27 | N10 |
| R11 | VSSQ-28 | VDDQ-28 | N5 |
| R12 | VSSQ-29 | VDDQ-29 | P1 |
| R14 | VSSQ-30 | VDDQ-30 | P12 |
| R3 | VSSQ-31 | VDDQ-31 | P14 |
| R4 | VSSQ-32 | VDDQ-32 | P3 |
| U1 | VSSQ-33 | VDDQ-33 | T1 |
| U12 | VSSQ-34 | VDDQ-34 | T12 |
| U14 | VSSQ-35 | VDDQ-35 | T14 |
| U3 | VSSQ-36 | VDDQ-36 | T3 |

K4G80325FB-HC25

GND

FBVDDQ

C569 C10u4X60603, C568 C10u4X60603, C636 C10u4X60603, C657 C10u4X60603

GND

C434 C10u4X60603, C501 C10u4X60603

GND

C87 C22u4X60603, C529 C22u4X60603, C727 C22u4X60603, C86 C22u4X60603, C97 C22u4X60603

GND

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DECOUPLING AROUND FBC MEMORIES (DQ32-DQ63)

FBVDDQ

SPARE

C743 C1u6.3X60402-RH, C534 C1u6.3X60402-RH, C70 C1u6.3X60402-RH, C91 C1u6.3X60402-RH, C539 C1u6.3X60402-RH, C538 C1u6.3X60402-RH, C65 C1u6.3X60402-RH, C751 C1u6.3X60402-RH, C66 C1u6.3X60402-RH, C69 C1u6.3X60402-RH, C469 C1u6.3X60402-RH, C646 C1u6.3X60402-RH, C701 C1u6.3X60402-RH, C459 C1u6.3X60402-RH, C759 C1u6.3X60402-RH, C752 C1u6.3X60402-RH, C758 C1u6.3X60402-RH, C749 C1u6.3X60402-RH

GND

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Title: DGPU_GDDR5 FB-C_DECOUPLING

Size: A3 | Document Number: MS-16K51 | Rev: 0B

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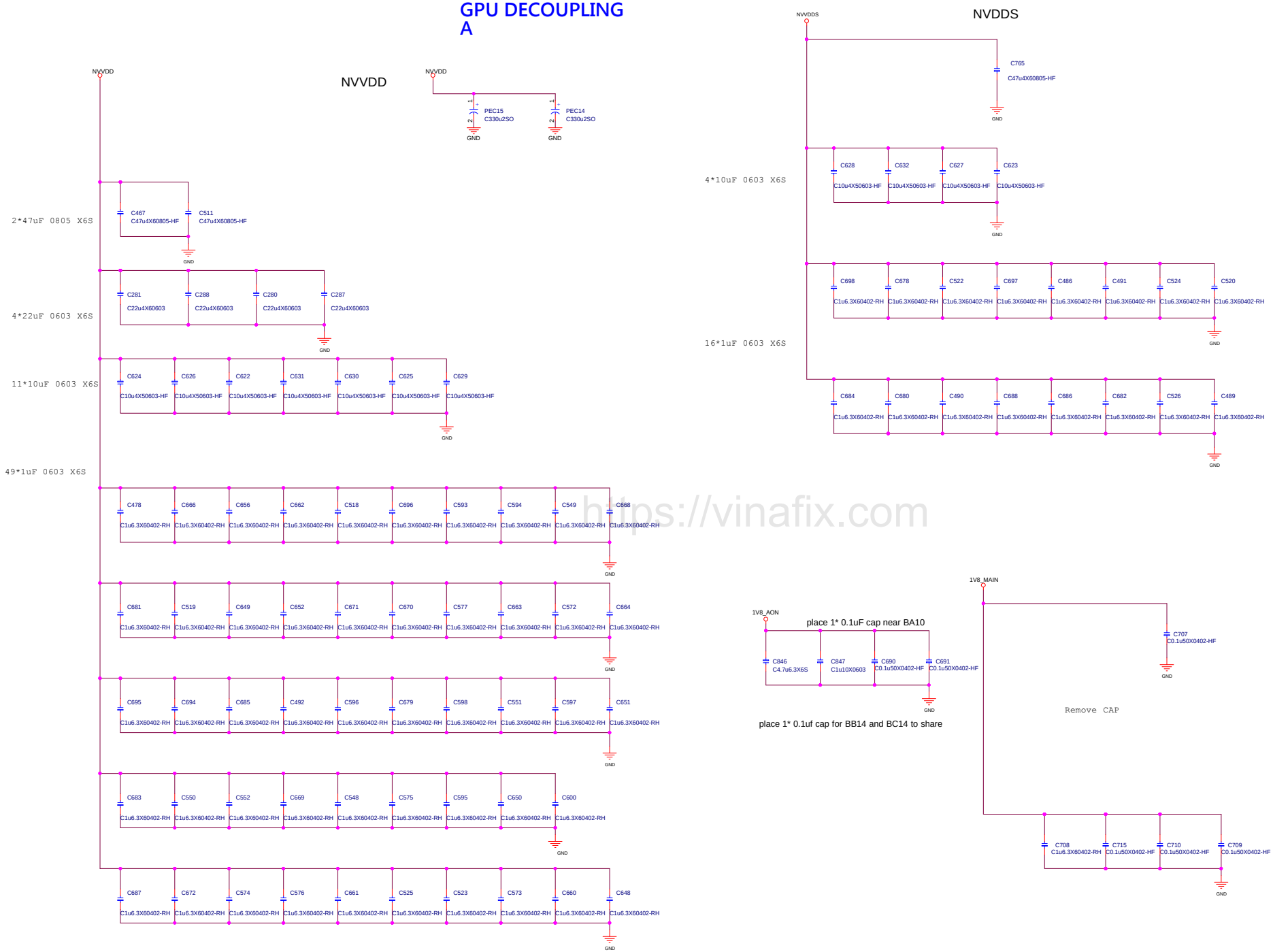
# GPU DECOUPLING A







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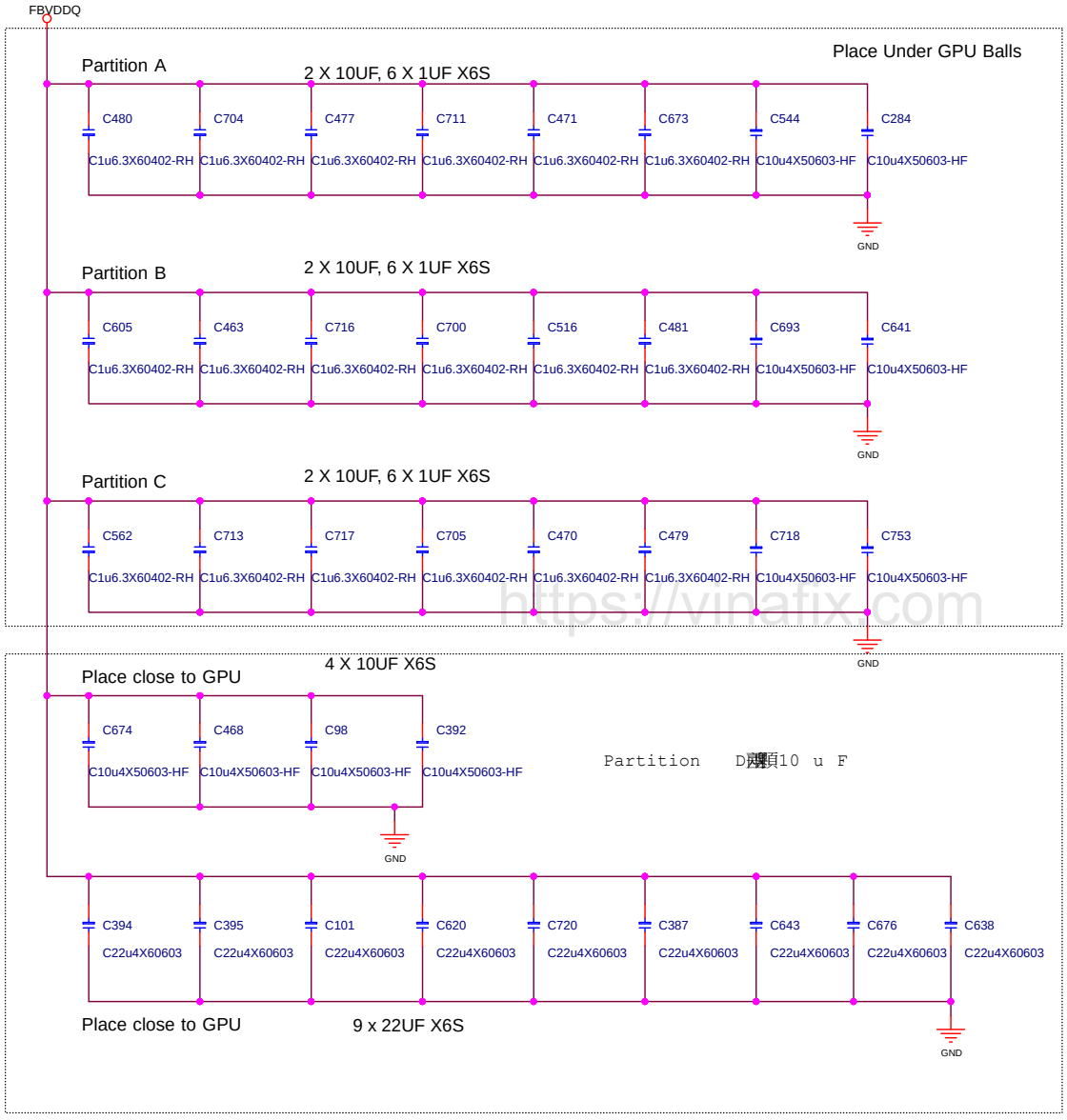
place 1* 0.1uf cap for BB14 and BC14 to share

| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | |
| Title: DGPU_GPU DECOUPLING A | | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B |
| Date: Thursday, October 05, 2017 | Sheet 23 of 80 | |

# GPU DECOUPLING B

## FBVDDQ

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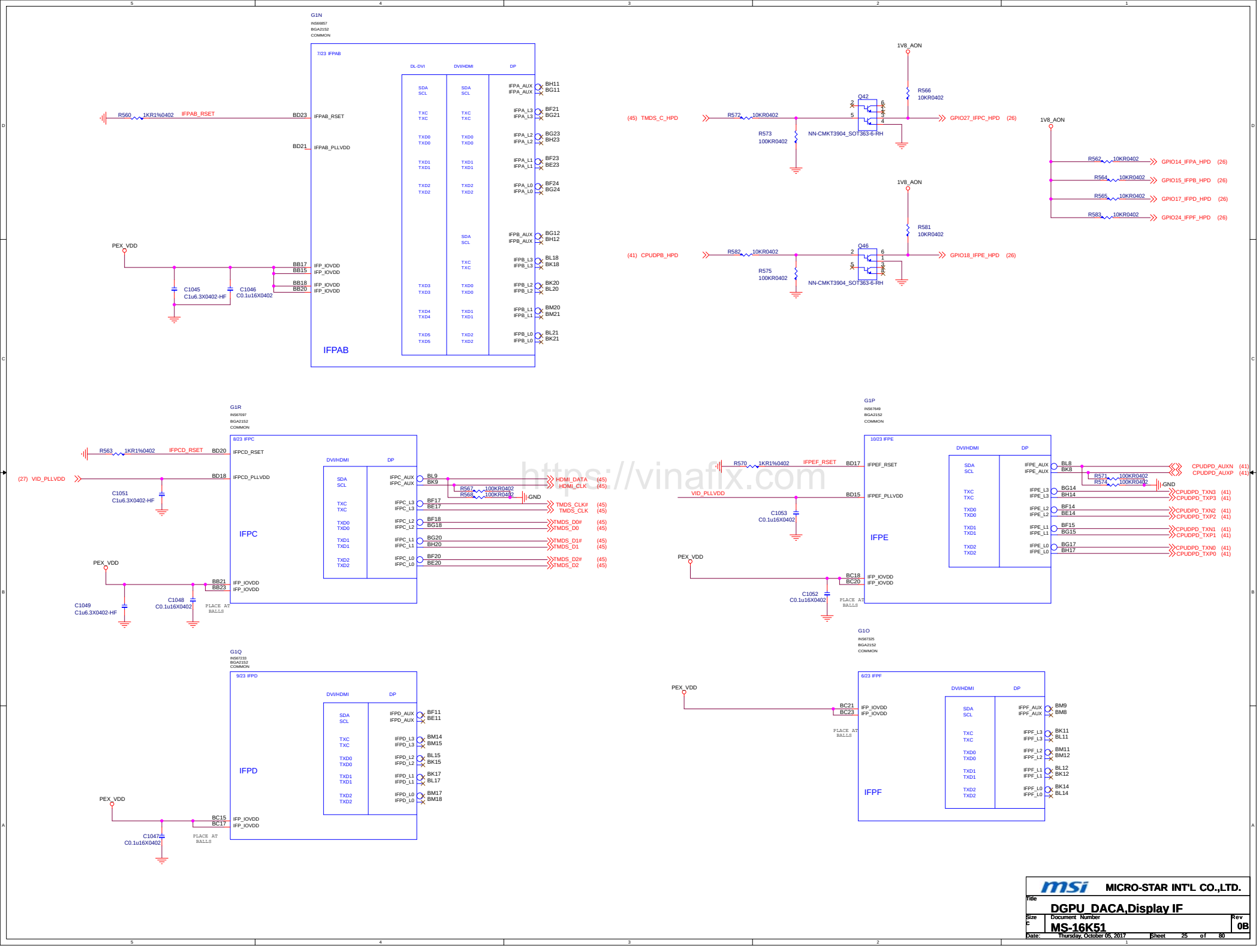
| | | |
|---|---|---|
| Title | DGPU GPU DECOUPLING B | |
| Size B | Document Number MS-16K51 | Rev 0B |
| Date: Thursday, October 05, 2017 | Sheet 24 of 80 | |

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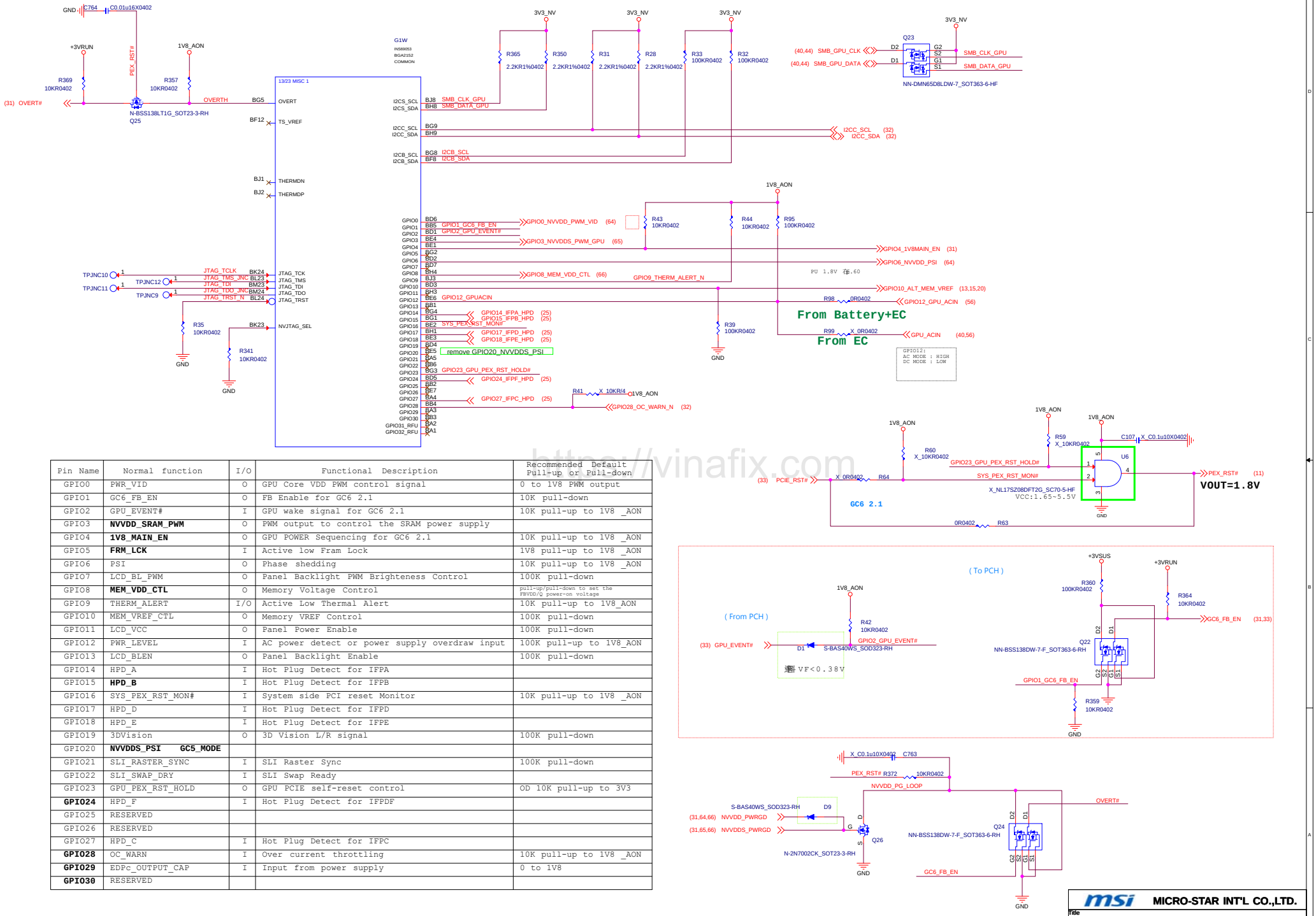
Title: DGPU_DACA,Display IF

Size: C | Document Number: MS-16K51 | Rev: 0B

Date: Thursday, October 05, 2017 | Sheet 25 of 80

# DGPU GPIO, I2C




| Pin Name | Normal function | I/O | Functional Description | Recommended Default Pull-up or Pull-down |
|---|---|---|---|---|
| GPIO0 | PWR_VID | O | GPU Core VDD PWM control signal | 0 to 1V8 PWM output |
| GPIO1 | GC6_FB_EN | O | FB Enable for GC6 2.1 | 10K pull-down |
| GPIO2 | GPU_EVENT# | I | GPU wake signal for GC6 2.1 | 10K pull-up to 1V8 _AON |
| GPIO3 | **NVVDD_SRAM_PWM** | O | PWM output to control the SRAM power supply | |
| GPIO4 | **1V8_MAIN_EN** | O | GPU POWER Sequencing for GC6 2.1 | 10K pull-up to 1V8 _AON |
| GPIO5 | **FRM_LCK** | I | Active low Fram Lock | 1V8 pull-up to 1V8 _AON |
| GPIO6 | PSI | O | Phase shedding | 10K pull-up to 1V8 _AON |
| GPIO7 | LCD_BL_PWM | O | Panel Backlight PWM Brighteness Control | 100K pull-down |
| GPIO8 | **MEM_VDD_CTL** | O | Memory Voltage Control | pull-up/pull-down to set the FBVDD/Q power-on voltage |
| GPIO9 | THERM_ALERT | I/O | Active Low Thermal Alert | 10K pull-up to 1V8_AON |
| GPIO10 | MEM_VREF_CTL | O | Memory VREF Control | 100K pull-down |
| GPIO11 | LCD_VCC | O | Panel Power Enable | 100K pull-down |
| GPIO12 | PWR_LEVEL | I | AC power detect or power supply overdraw input | 100K pull-up to 1V8_AON |
| GPIO13 | LCD_BLEN | O | Panel Backlight Enable | 100K pull-down |
| GPIO14 | HPD_A | I | Hot Plug Detect for IFPA | |
| GPIO15 | **HPD_B** | I | Hot Plug Detect for IFPB | |
| GPIO16 | SYS_PEX_RST_MON# | I | System side PCI reset Monitor | 10K pull-up to 1V8 _AON |
| GPIO17 | HPD_D | I | Hot Plug Detect for IFPD | |
| GPIO18 | HPD_E | I | Hot Plug Detect for IFPE | |
| GPIO19 | 3DVision | O | 3D Vision L/R signal | 100K pull-down |
| GPIO20 | **NVVDDS_PSI GC5_MODE** | | | |
| GPIO21 | SLI_RASTER_SYNC | I | SLI Raster Sync | 100K pull-down |
| GPIO22 | SLI_SWAP_DRY | I | SLI Swap Ready | |
| GPIO23 | GPU_PEX_RST_HOLD | O | GPU PCIE self-reset control | OD 10K pull-up to 3V3 |
| **GPIO24** | HPD_F | I | Hot Plug Detect for IFPDF | |
| GPIO25 | RESERVED | | | |
| GPIO26 | RESERVED | | | |
| GPIO27 | HPD_C | I | Hot Plug Detect for IFPC | |
| **GPIO28** | OC_WARN | I | Over current throttling | 10K pull-up to 1V8 _AON |
| **GPIO29** | EDPc_OUTPUT_CAP | I | Input from power supply | 0 to 1V8 |
| **GPIO30** | RESERVED | | | |

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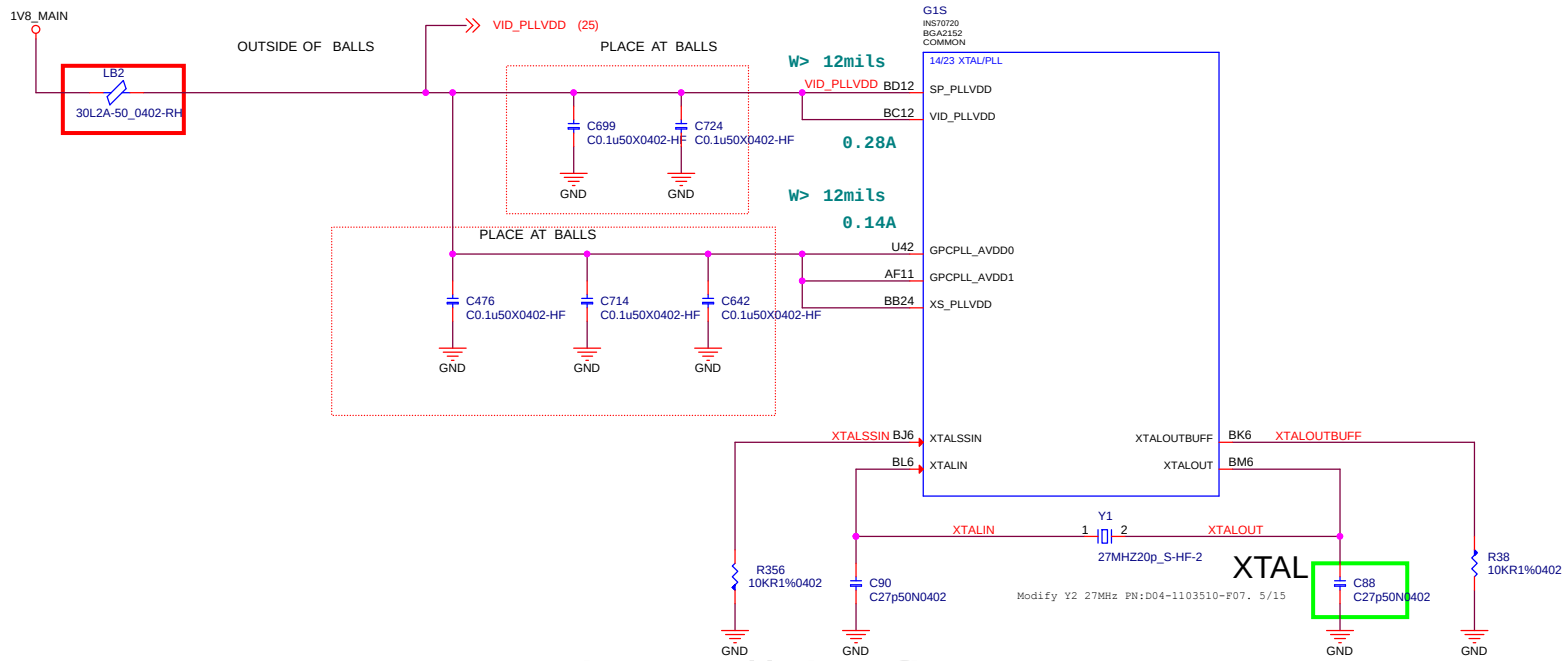
| | | |
|---|---|---|
| Title | DGPU_GPIO,I2C | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B |
| Date: Thursday, October 05, 2017 | Sheet 26 of 80 | |

# DGPU MIO & XTAL

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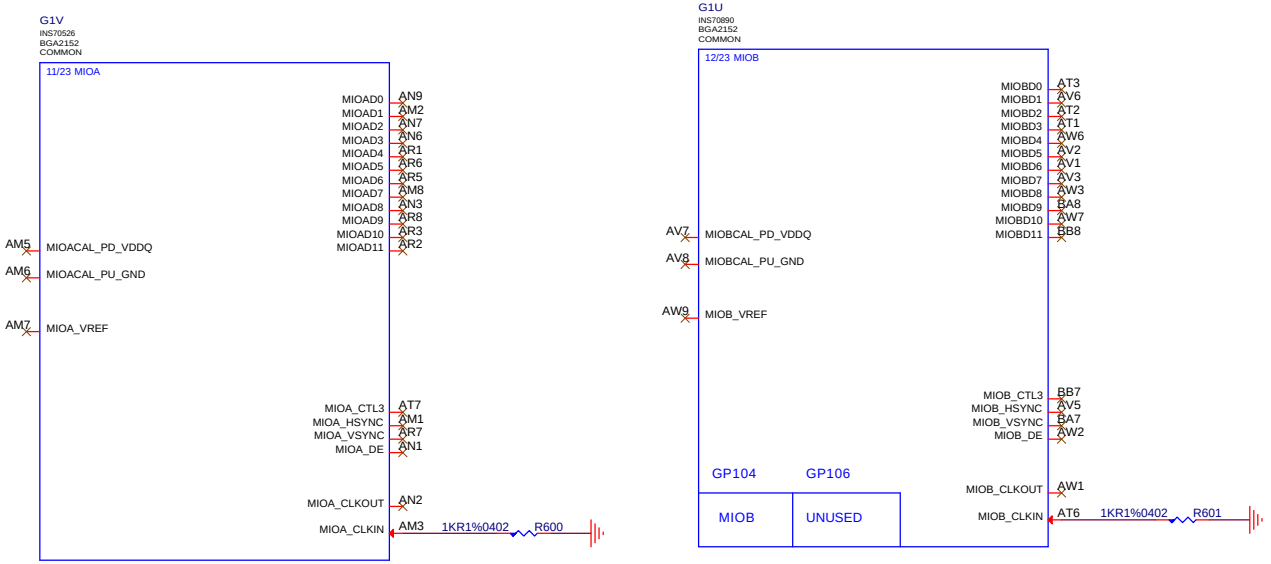
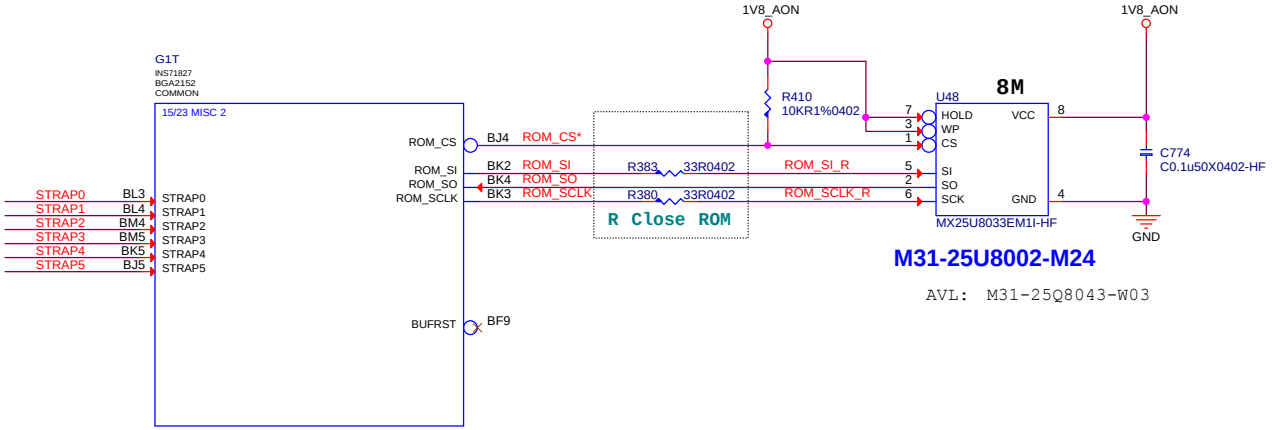
## Multi-use IO(MIO) Interface

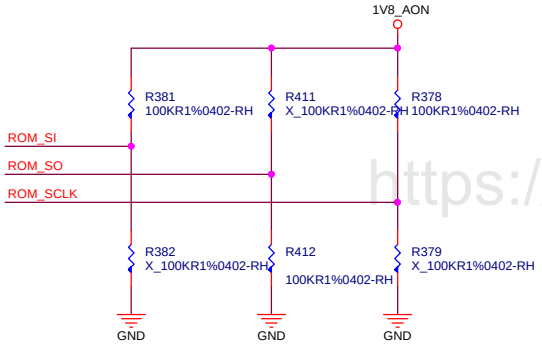



| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | |
| Title: DGPU MIO & XTAL | | |
| Size: A3 | Document Number: MS-16K51 | Rev: 0B |
| Date: Thursday, October 05, 2017 | Sheet 27 of 80 | |

# ROM



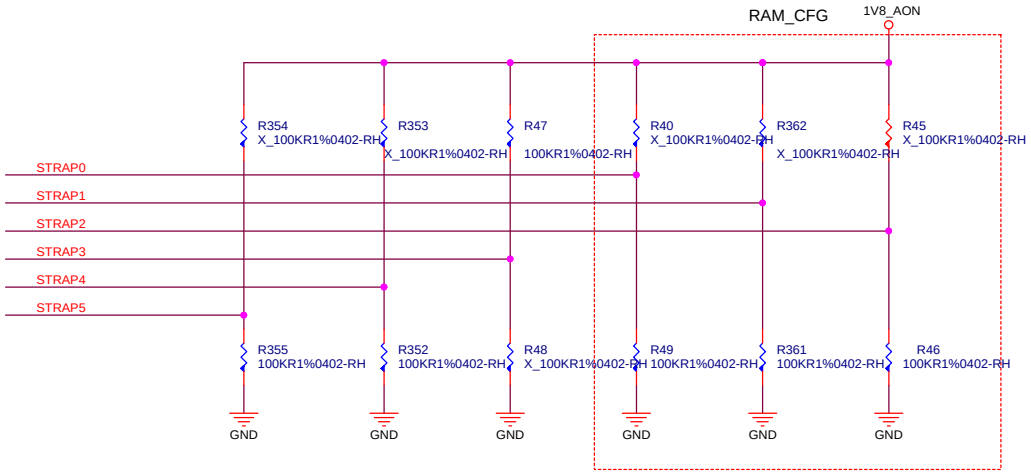

# MULTI-LEVEL STRAPS




https://vinafix.com

| STRAP2 | STRAP1 | STRAP0 | RAMCFG[4:0] |
|---|---|---|---|
| L | L | L | 00000 |
| L | L | H | 00001 |
| L | H | L | 00010 |
| L | H | H | 00011 |
| H | H | L | 00110 |
| H | H | H | 00111 |

256M*32
SAMSUNG 0X0
MICRON 0X1




DEFAULT SETTING

V_TOP1
5010
M12-8032535-S02
X_K4G80325FB-HC25
Samsung
256M*32

V_TOP2
5010
M12-2563215-M30
X_MT51J256M32HF-80:A
Micron
256M*32

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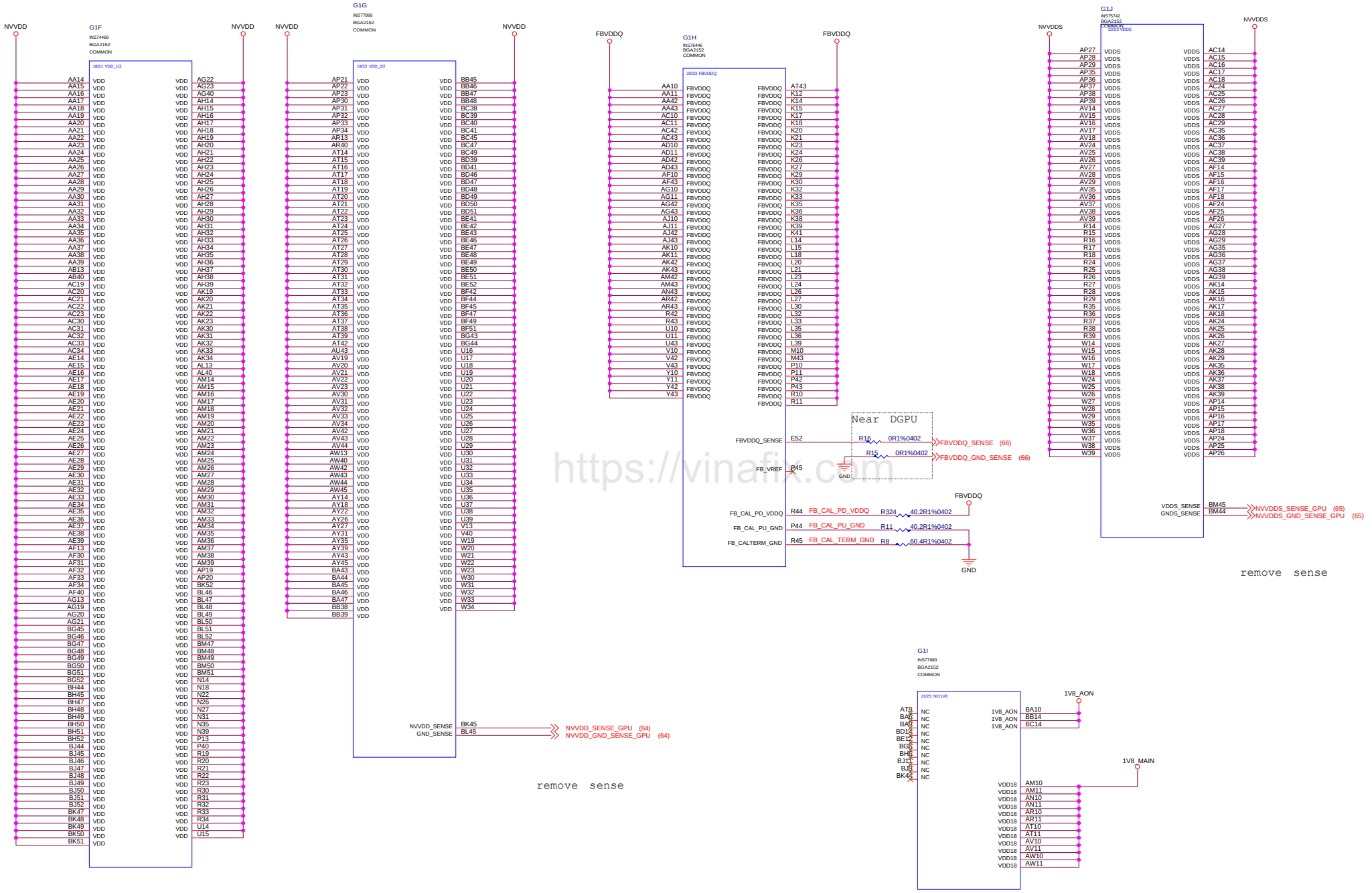
Title: DGPU_ROM,HW Straps

Size: Custom | Document Number: MS-16K51 | Rev: 0B

Date: Thursday, October 05, 2017 | Sheet 28 of 80

# GPU NVVDD, FBVDDQ

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| | |
|---|---|
| Title | DGPU NVVDD, FBVDDQ |
| Size | Custom |
| Document Number | MS-16K51 |
| Rev | 0B |
| Date | Thursday, October 05, 2017 |
| Sheet | 29 of 80 |

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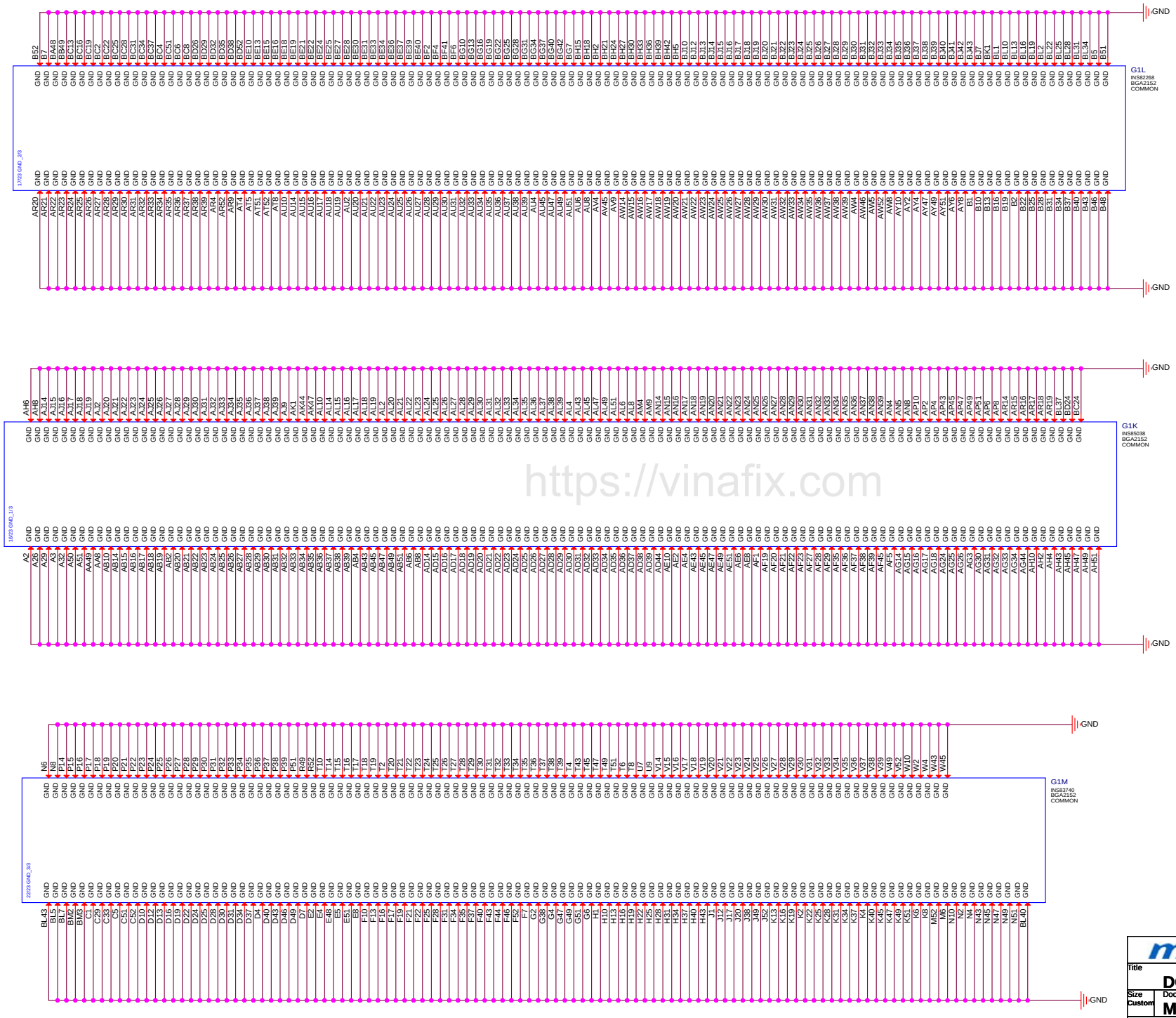
# DGPU GND




| | | | |
|---|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | | |
| Title: DGPU GND | | | |
| Size: Custom | Document Number: MS-16K51 | | Rev: 0B |
| Date: Tuesday, October 03, 2017 | Sheet 30 of 80 | | |

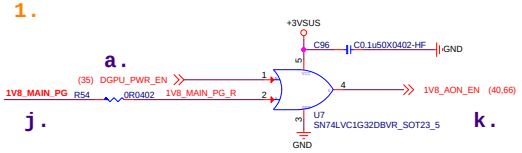
# nVIDIA Power Sequence Control

**Power on = 1V8_AON ->1V8_MAIN->3V3_NV -> NVVDD ->NVVDDS/PEX_VDD -> FBVDDQ -> DGPUPWRGD**

**Power off= DGPUPWREN->(NVVDDS->PEX_VDD->FBVDDQ)->(NVVDD->3V3_NV)->1V8_MAIN->1V8_AON**

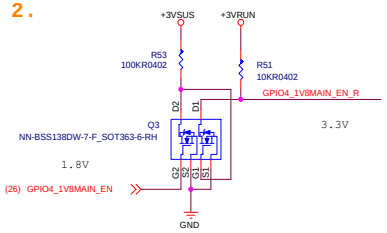
1.

a.

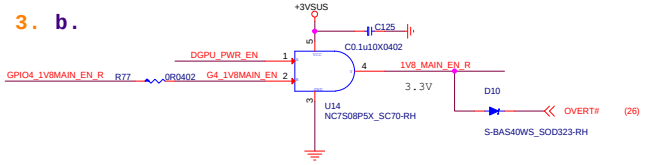



j. k.

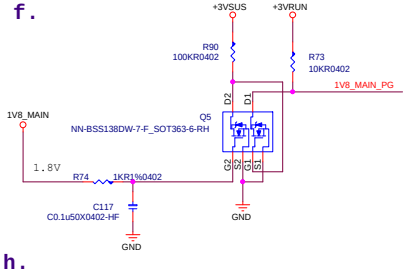
2.



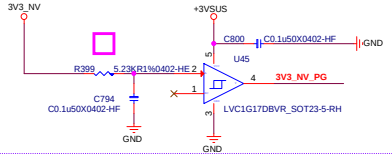

3. b.



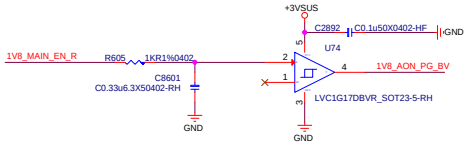

5. f.



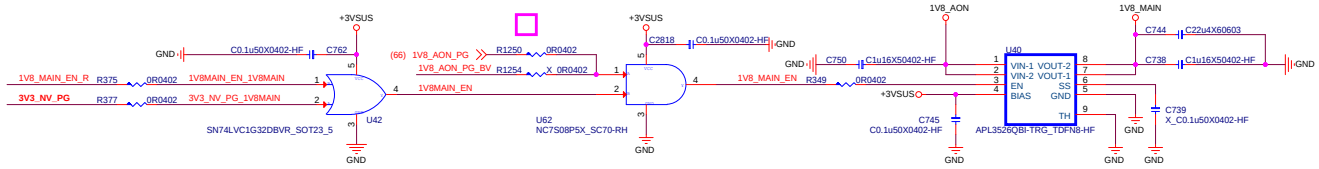

7. h.



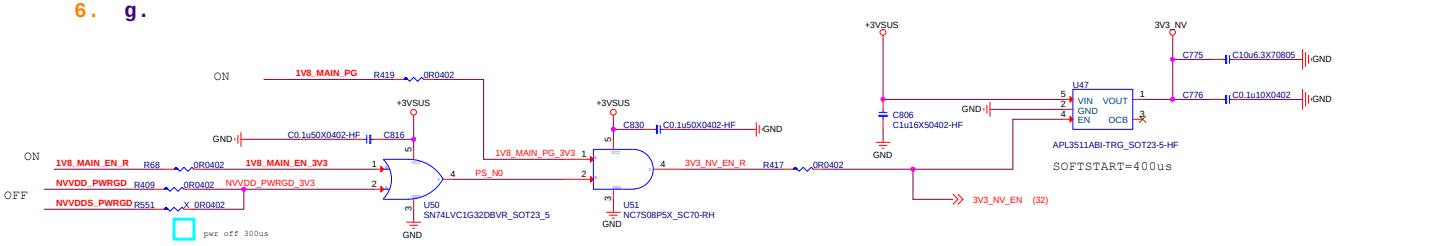

**1V8_AON Power Good By Voltage and delay**



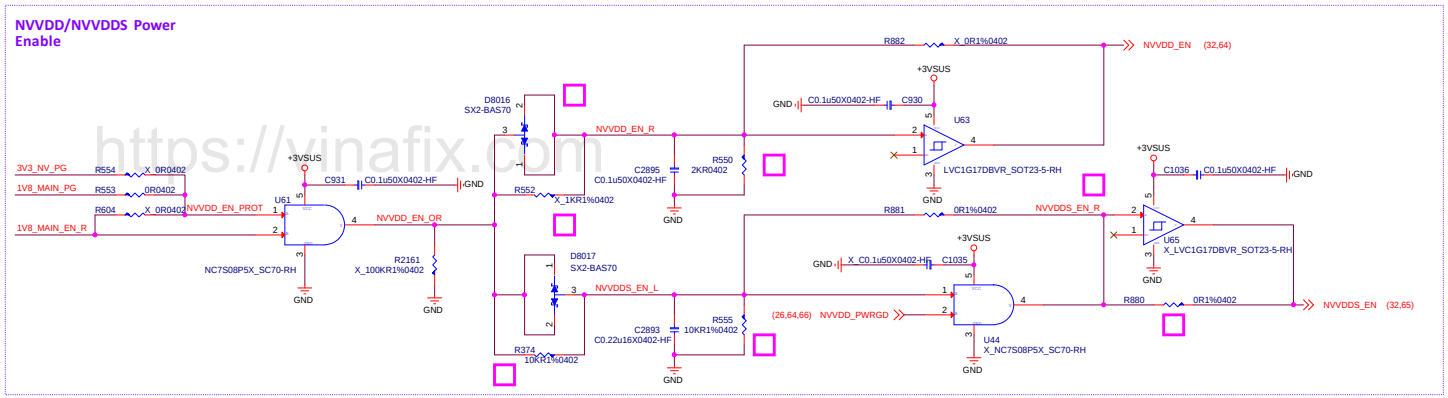

4. i.




6. g.




**NVVDD/NVVDDS Power Enable**

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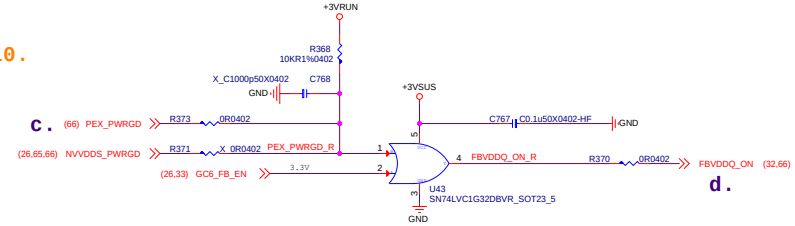
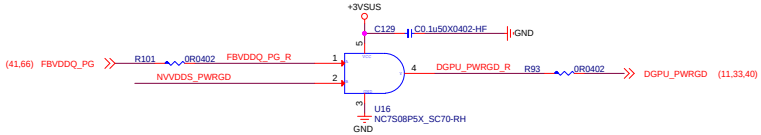
10.

c.




d.

11.

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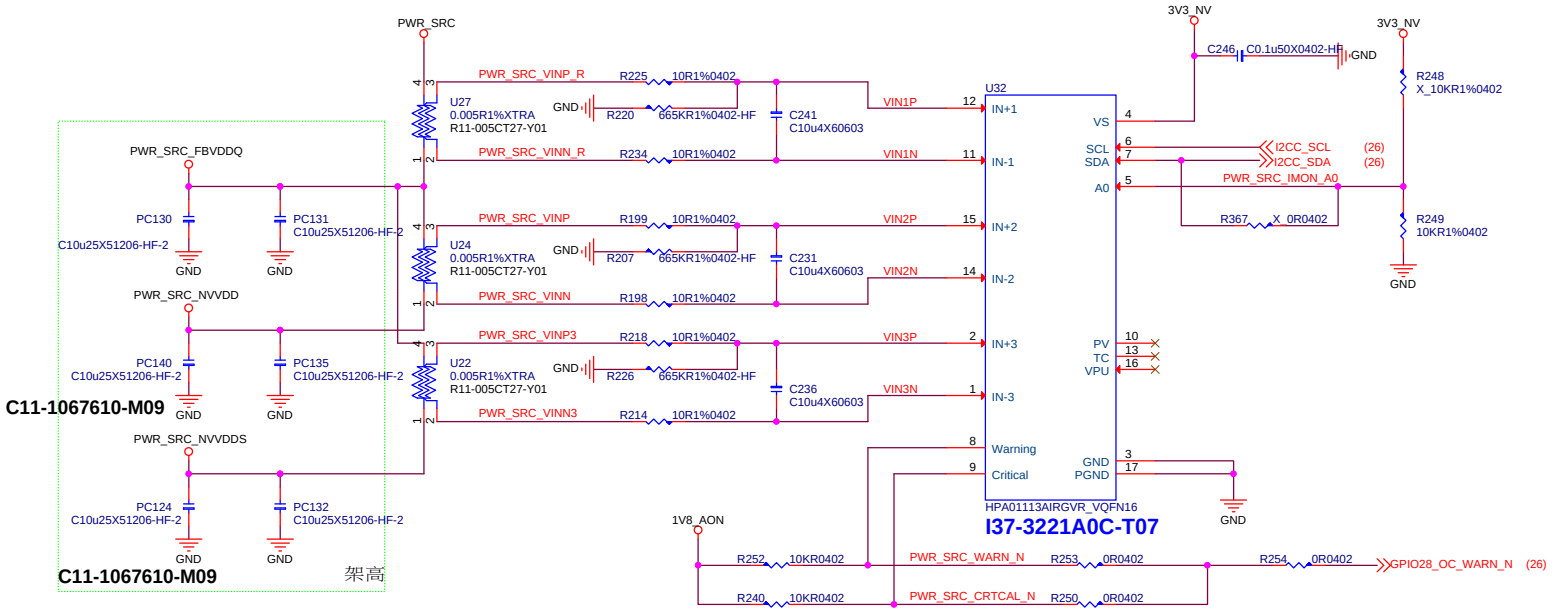
Title: DGPU_Power Sequence

Size | Document Number: MS-16K51 | Rev: 0B

Date: | Sheet 31 of 80

# DGPU_Power Control

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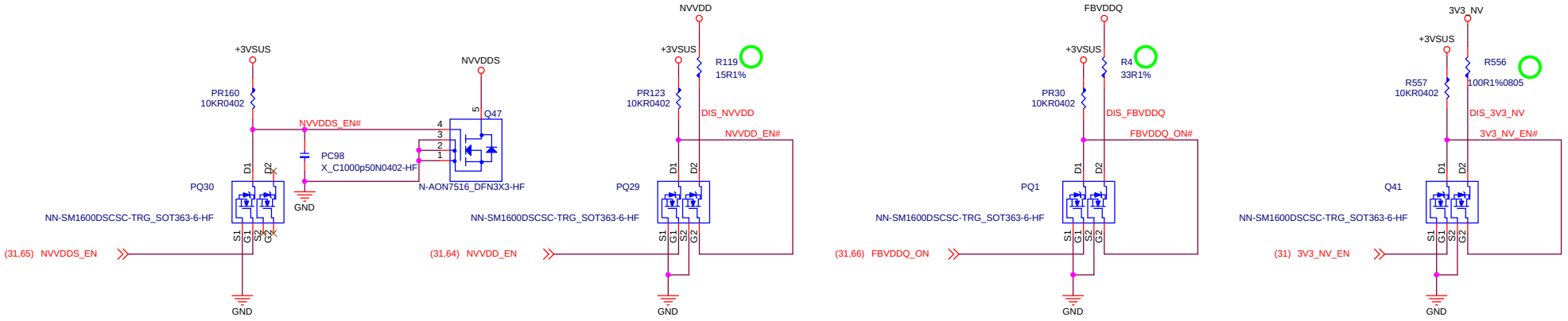
# Discharge




PEX_VDD 放電 4 ms

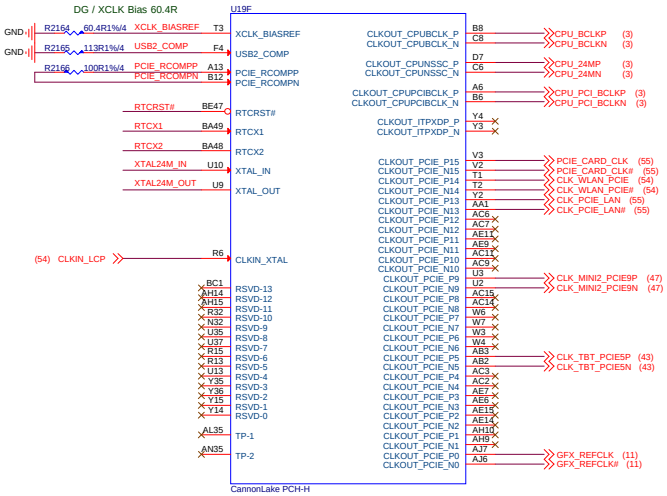
3V3_AON 放電 2 ms

1V8AON 放電 2ms

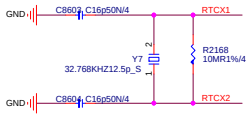
1V8_MAIN 放電 320 us

| | | | |
|---|---|---|---|
| msi MICRO-STAR INT'L CO.,LTD. | | | |
| Title: DGPU_Discharge | | | |
| Size: Custom | Document Number: MS-16K51 | | Rev: 0B |
| Date: Friday, October 13, 2017 | Sheet 32 of 80 | | |

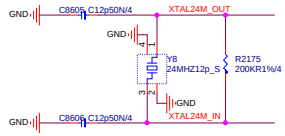
# HM370 (RTC/PCIE_Clock/Clock/RSVD)



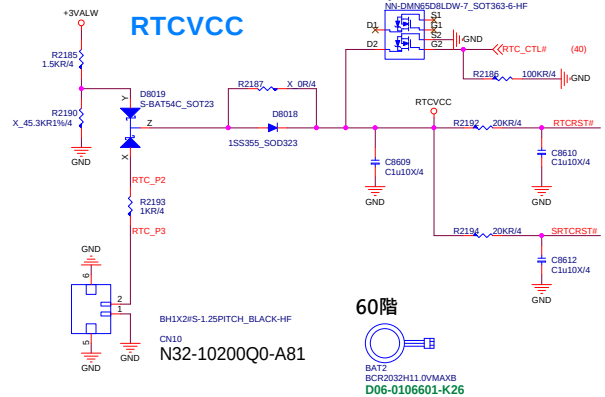

## RTC Block(Close to PCH)



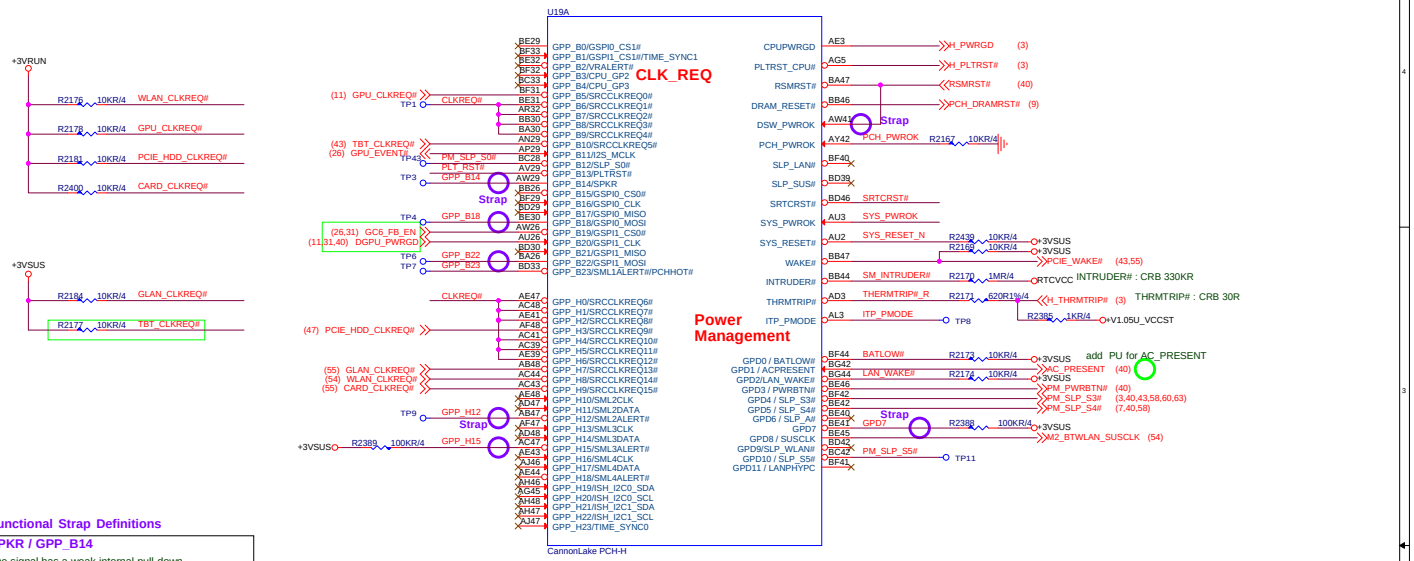

## 24MHz Clock




## RTCVCC




# HM370 (CLKREQ/ACPI)




## Functional Strap Definitions

**SPKR / GPP_B14**

The signal has a weak internal pull-down.
0 = Disable Top Swap mode. (Default)

**GSPI0_MOSI / GPP_B18**

The signal has a weak internal pull-down.
0 = Disable No Reboot mode. (Default)
1 = Enable No Reboot mode

**GSPI1_MOSI / GPP_B22**

This Signal has a weak internal pull-down.

| Bit 6 Boot BIOS | Destination |
|---|---|
| 0 | SPI (Default) |
| 1 | LPC |

**SML1ALERT# / PCHHOT#/ GPP_B23**

This signal has an internal pull-down.

**GPP_H12**

This signal has a weak internal pull-down.

**GPP_H15**

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

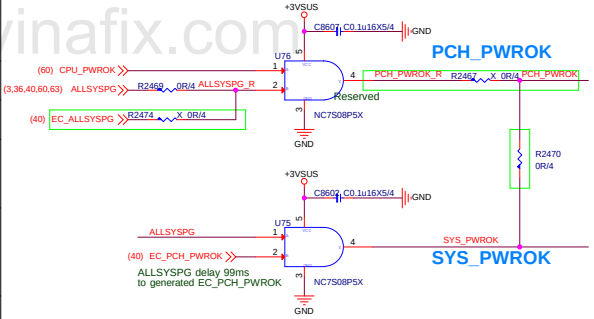
**GPPD7**

External pull-up is required. Recommend 100K.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

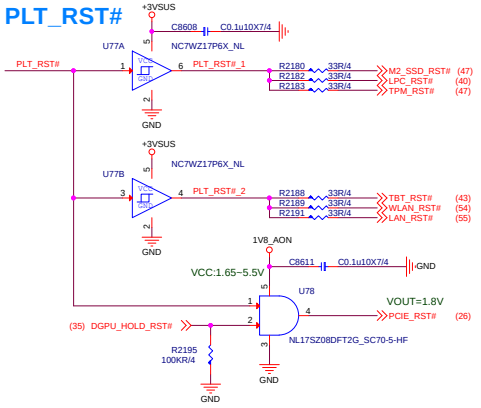
**DG/ RTC Well Input Strap**

RSMRST# & DSW_PWROK, PCH_PWROK : PD
RTCRST#, SRTCRST#, INTRUDER# : PU

## PCH_PWROK




## PLT_RST#

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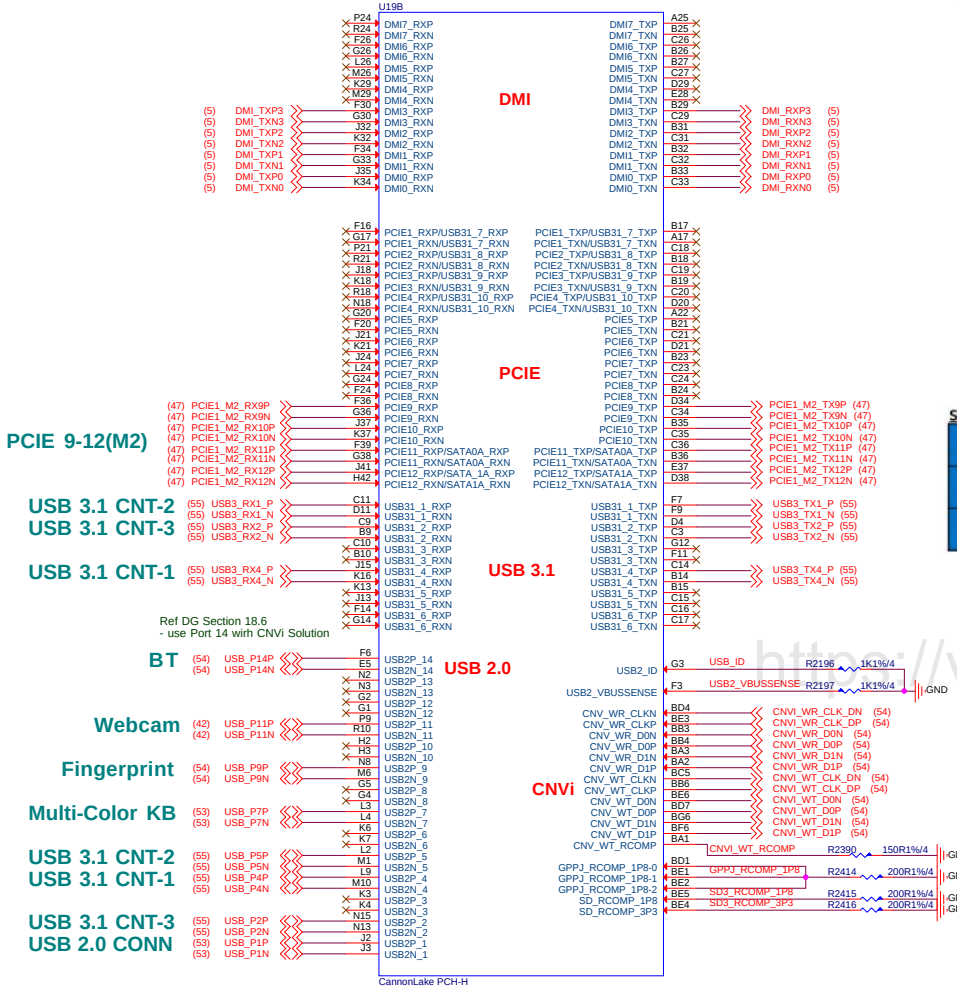
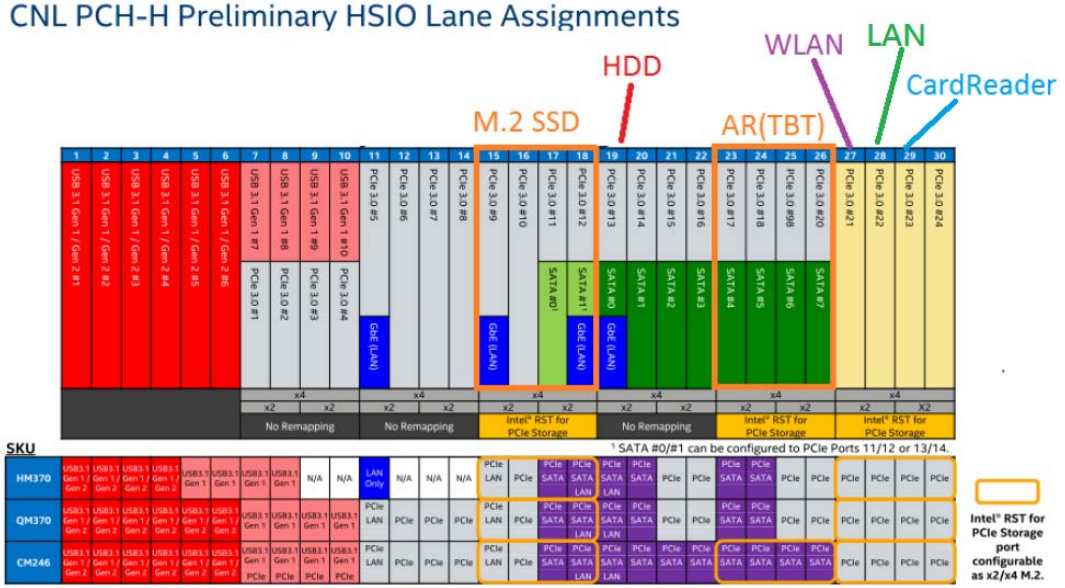
| | | |
|---|---|---|
| msi | MICRO-STAR INT'L CO.,LTD. | |
| Title | PCH-1(CLK,ACPI) | |
| Size | Document Number: MS-16K51 | Rev: 0B |
| Date: Friday, October 13, 2017 | Sheet 33 of 80 | |

# HM370 (DMI/PCIE/USB3.1/USB2.0/CNVi)




# CNL PCH-H Preliminary HSIO Lane Assignments




SKU

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| HM370 | USB3.1 Gen 1 / Gen 2 #1 | USB3.1 Gen 1 / Gen 2 #2 | USB3.1 Gen 1 / Gen 2 #3 | USB3.1 Gen 1 / Gen 2 #4 | USB3.1 Gen 1 / Gen 2 #5 | USB3.1 Gen 1 / Gen 2 #6 | USB3.1 Gen 1 #7 | USB3.1 Gen 1 #8 | USB3.1 Gen 1 #9 | USB3.1 Gen 1 #10 | LAN Only | N/A | N/A | N/A | PCIe LAN | PCIe | PCIe SATA LAN | PCIe SATA LAN | PCIe SATA LAN | PCIe SATA | PCIe | PCIe | PCIe SATA | PCIe SATA | PCIe | PCIe | PCIe | PCIe | PCIe | PCIe |
| QM370 | USB3.1 Gen 1 / Gen 2 | USB3.1 Gen 1 / Gen 2 | USB3.1 Gen 1 / Gen 2 | USB3.1 Gen 1 / Gen 2 | USB3.1 Gen 1 / Gen 2 | USB3.1 Gen 1 / Gen 2 | USB3.1 Gen 1 | USB3.1 Gen 1 | USB3.1 Gen 1 | USB3.1 Gen 1 | PCIe LAN | PCIe | PCIe | PCIe | PCIe LAN | PCIe | PCIe SATA LAN | PCIe SATA LAN | PCIe SATA LAN | PCIe SATA | PCIe | PCIe | PCIe SATA | PCIe SATA | PCIe | PCIe | PCIe | PCIe | PCIe | PCIe |
| CM246 | USB3.1 Gen 1 / Gen 2 | USB3.1 Gen 1 / Gen 2 | USB3.1 Gen 1 / Gen 2 | USB3.1 Gen 1 / Gen 2 | USB3.1 Gen 1 / Gen 2 | USB3.1 Gen 1 / Gen 2 | USB3.1 Gen 1 | USB3.1 Gen 1 | USB3.1 Gen 1 | USB3.1 Gen 1 | PCIe LAN | PCIe | PCIe | PCIe | PCIe LAN | PCIe | PCIe SATA LAN | PCIe SATA LAN | PCIe SATA LAN | PCIe SATA | PCIe | PCIe | PCIe SATA | PCIe SATA | PCIe SATA | PCIe SATA | PCIe | PCIe | PCIe | PCIe |

[1] SATA #0/#1 can be configured to PCIe Ports 11/12 or 13/14.

Intel® RST for PCIe Storage port configurable as x2/x4 M.2.

- Added 4 new PCIe 3.0 lanes versus KBL-H platform.
- GbE LAN removed from lane 10 and SATA #0/#1 option moved from lanes 15/16 to 19/20 to better balance PHY clocking.

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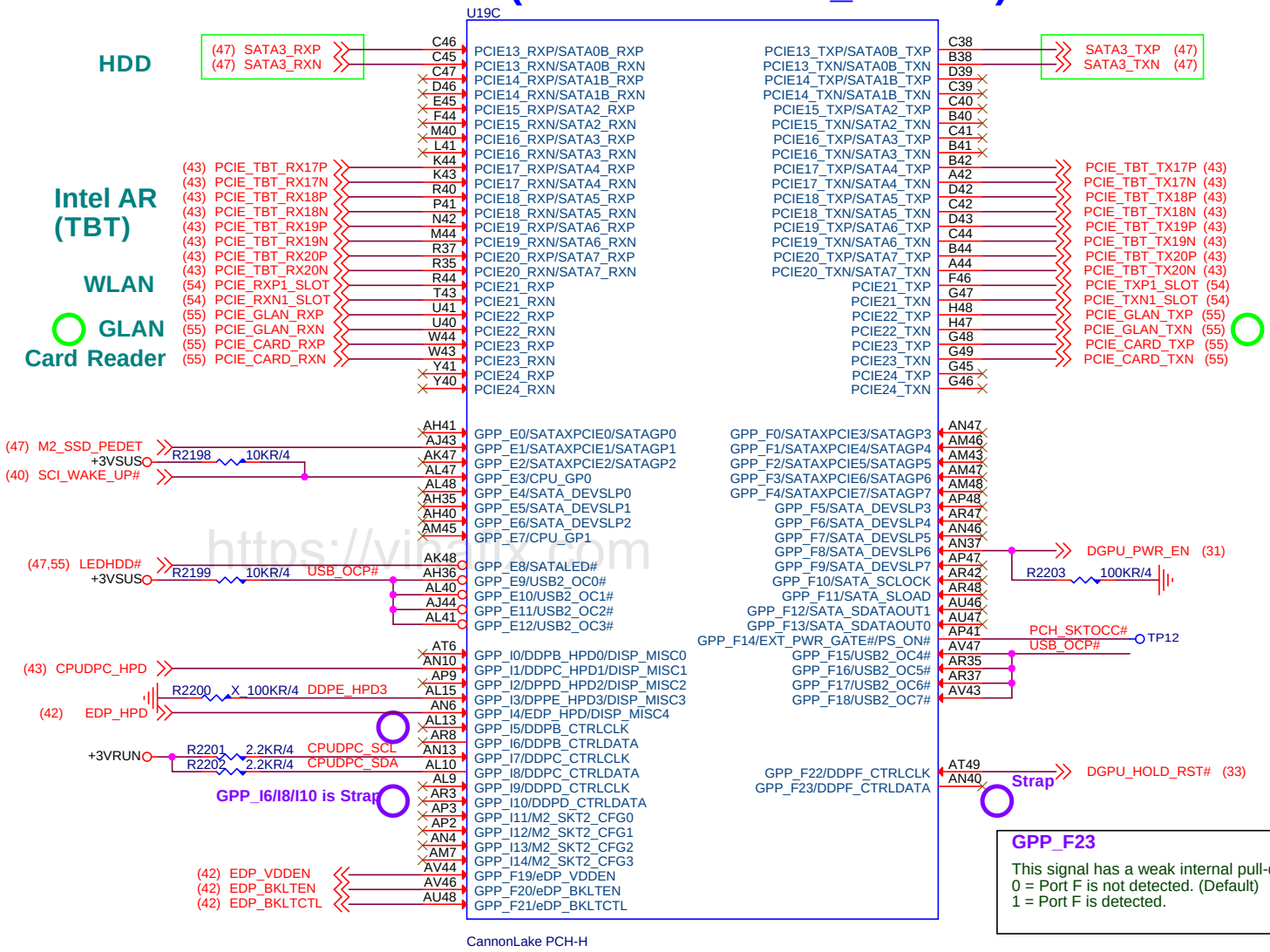
MICRO-STAR INT'L CO.,LTD.

Title: PCH-2(DMI/PCIE/USB)

Size | Document Number: MS-16K51 | Rev: 0B

Date: Thursday, October 05, 2017 | Sheet 34 of 80

# HM370(SATA/PCIE/USB_OC/DDI)




## Functional Strap Definitions

### DDPB_CTRLDATA / GPP_I6

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

### DDPC_CTRLDATA / GPP_I8

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

### DDPD_CTRLDATA / GPP_I10

This signal has a weak internal pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.

### GPP_F23

This signal has a weak internal pull-down.
0 = Port F is not detected. (Default)
1 = Port F is detected.

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MICRO-STAR INT'L CO.,LTD.

Title: PCH-3(SATA/PCIE/USB_OC/DDI)

Size: Custom | Document Number: MS-16K51 | Rev: 0B

Date: Thursday, October 05, 2017 | Sheet 35 of 80

# HM370 (HDA/GPIO/TJAG)

## Functional Strap Definitions

**SMBALERT# / GPP_C2**

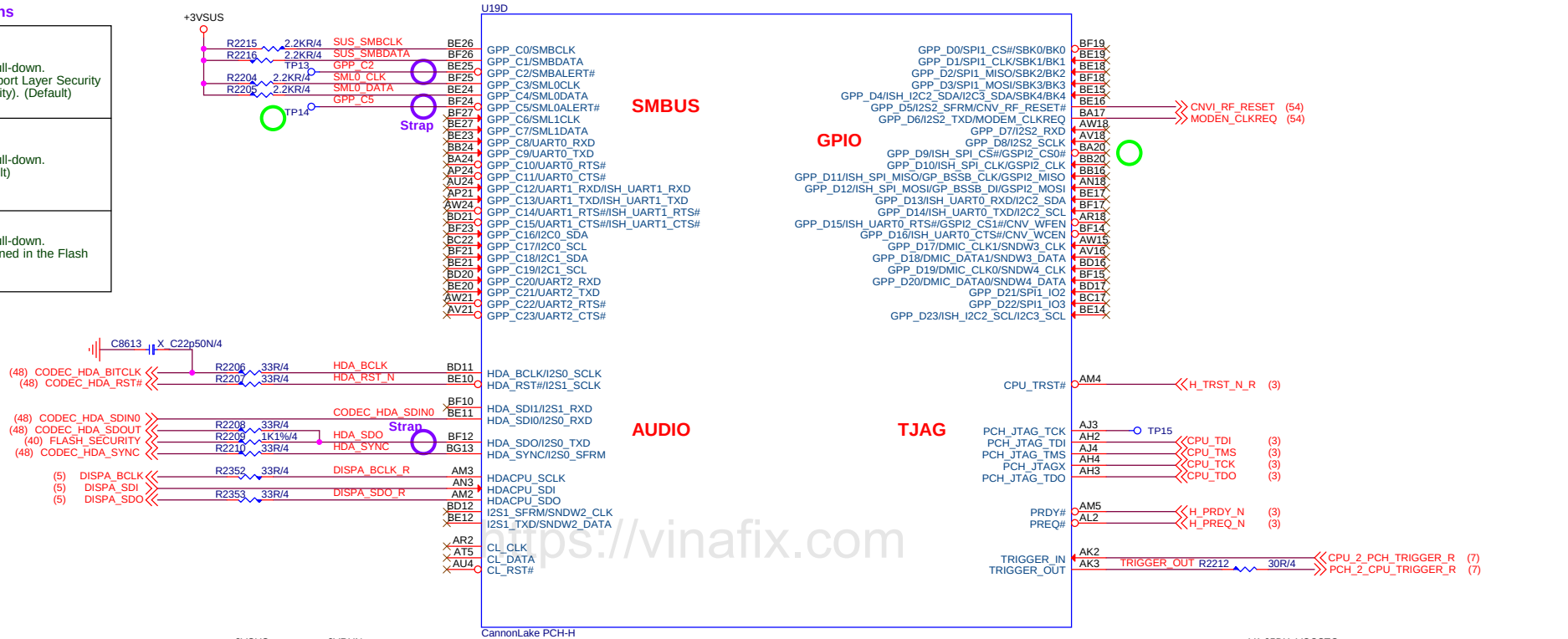
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

**SML0ALERT# / GPP_C5**

This signal has a weak internal pull-down.
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.

**HDA_SDO**

This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)

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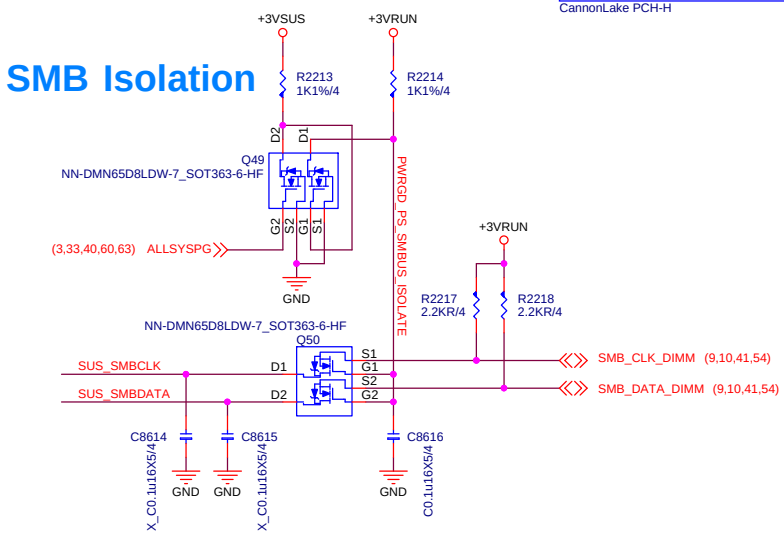
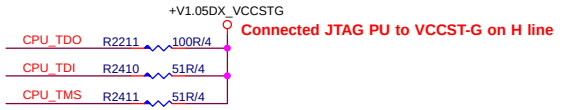
## SMB Isolation




**Connected JTAG PU to VCCST-G on H line**

ref DG / Chapter Platform and Test Hooks
CPU_TDO : PU 100R Near CPU (DG : R1)
PU 100R Near PCH (DG : R3)
CPU_TDI : PU 51R Near PCH (DG : R4)
CPU_TMS : PU 51R Near PCH (DG : R5)
CPU_TCK : 51R to GND Near CPU (DG : R2)

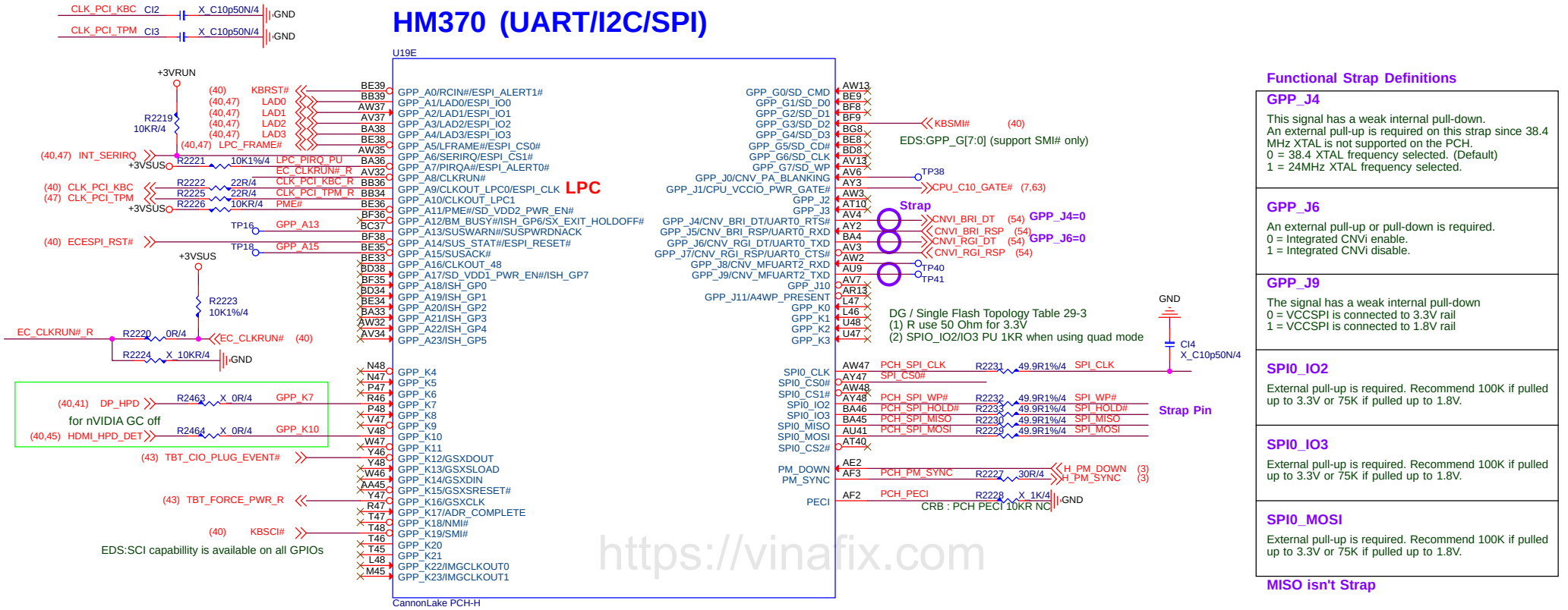
MICRO-STAR INT'L CO.,LTD.

Title: PCH-4(HDA/GPIO/TJAG)

Size: Custom | Document Number: MS-16K51 | Rev: 0B

Date: Thursday, October 05, 2017 | Sheet 36 of 80

# HM370 (UART/I2C/SPI)

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## Functional Strap Definitions

**GPP_J4**

This signal has a weak internal pull-down.
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.

**GPP_J6**

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

**GPP_J9**

The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

**SPI0_IO2**

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

**SPI0_IO3**

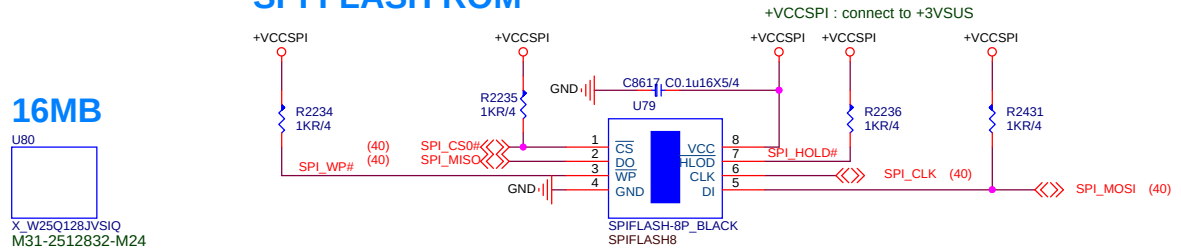
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

**SPI0_MOSI**

External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.

**MISO isn't Strap**

# SPI FLASH ROM



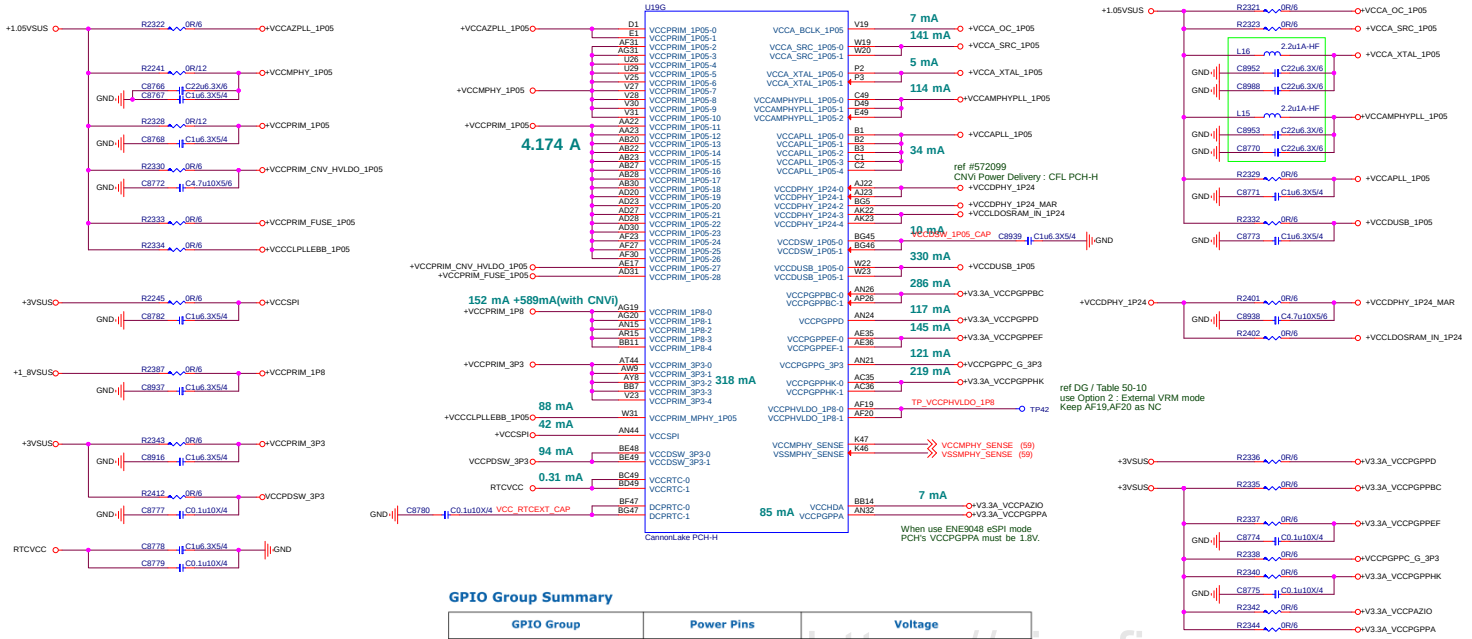

M31-2512893-W03
,M-IC FLASH,128M(16Mx8bit),10ms,SOIC-8pin(208mil),WINBOND/W25Q128JVSIQ,2.7V,3.6V,SPI,,HALOGEN FREE

M31-2512832-M24
,M-IC FLASH,128M(16Mx8bit),40ms,SOP-8pin,MXICMX25L12873FM2I-10G(T),2.7V,3.6V,SPI,,HALOGEN FREE

| | |
|---|---|
| MICRO-STAR INT'L CO.,LTD. | |
| Title | PCH-5(UART/I2C/SPI) |
| Size | Document Number: MS-16K51 |
| Rev | 0B |
| Date: Friday, October 06, 2017 | Sheet 37 of 80 |

# HM370 (Power)

ref DG / Table 50-6 Decoupling Requirements




## GPIO Group Summary

| GPIO Group | Power Pins | Voltage |
|---|---|---|
| Primary Well Group A (GPP_A) | VCCPGPPA | 1.8V or 3.3V |
| Primary Well Group B (GPP_B)<br>Primary Well Group C (GPP_C) | VCCPGPPBC | 1.8V or 3.3V |
| Primary Well Group D (GPP_D) | VCCPGPPD | 1.8V or 3.3V |
| Primary Well Group E (GPP_E)<br>Primary Well Group F (GPP_F) | VCCPGPPEF | 1.8V or 3.3V |
| Primary Well Group G (GPP_G) | VCCPGPPG_3P3 or VCCPRIM_1P8 | 1.8V or 3.3V |
| Primary Well Group H (GPP_H)<br>Primary Well Group K (GPP_K) | VCCPGPPHK | 1.8V or 3.3V |
| Primary Well Group I (GPP_I) | VCCPRIM_3P3 | 3.3V Only |
| Primary Well Group J (GPP_J) | VCCPRIM_1P8 | 1.8V Only |
| Deep Sleep Well Group (GPD) | VCCDSW_3P3 | 3.3V Only |

***Note:*** Except for GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.

## Power Descriptions for PCH in CNL-H

| Name | Description |
|---|---|
| **VCCA_BCLK_1P05** | **Analog supply for BCLK circuitries**: 1.05V |
| **VCCA_SRC_1P05** | **Analog supply for PCIe clock circuitries**: 1.05V |
| **VCCA_XTAL_1P05** | **Analog supply for XTAL circuitries**: 1.05V |
| **VCCDUSB_1P05** | **Supply for USB digital logic**: 1.05V |
| **VCCAPLL_1P05** | **Analog supply for BCLK/DMI/Audio PLLs:** 1.05V. This rail can be derived from the VCCPRIM_1P05 rail with the proper isolation. Refer to the Platform Design Guide for implementation detail. |
| **VCCPRIM_1P05** | **Primary Well**: 1.05V. For PCIe//USB3/SATA MPHY logic, I/O blocks, SRAM, JTAG, CNVi. |
| **VCCDSW_1P05** | **Deep Sx Well**: 1.05V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic. Board needs to connect a 1uF capacitor to this rail and power should NOT be driven from the board. |
| **VCCPRIM_MPHY_1P05** | **Mod PHY Primary**: 1.05V. Primary supply for PCIe/USB3/SATA MPHY logic and PCIe/USB PLL dividers. |
| **VCCAMPHYPLL_1P05** | **Analog supply for USB3, PCIe Gen 2/Gen 3, and SATA3 PLLs**: 1.05V. Refer to the Platform Design Guide for filtering and decoupling recommendations. |
| **VCCPRIM_1P8** | **1.8V Primary Well**. |
| **VCCPRIM_3P3** | **3.3V Primary Well**. |
| **VCCSPI** | **SPI Primary Well 3.3V or 1.8V**, for SPI interface. |
| **VCCHDA** | **HDA Audio Power 3.3V, 1.8V, or 1.5V**, for Intel® High Definition Audio. |
| **VCCDSW_3P3** | **3.3V Deep Sx Well**. |
| **VCCRTC** | **RTC Well Supply**. This rail can drop to 2.0V if all other planes are off. This power is not expected to be shut off unless the RTC battery is removed or drained.<br>***Note:*** VCCRTC nominal voltage is 3.0V. This rail is intended to always come up first and always stay on. It should NOT be power cycled regularly on non-coin battery designs. Refer to the Platform Design Guide, RTC Design Guidelines chapter for latest design recommendations.<br>***Note:*** Implementation should not attempt to clear CMOS by using a jumper to pull VCCRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI. |
| **DCPRTC** | RTC decoupling capacitor only. This rail should NOT be driven. |
| **VCCDPHY_1P24** | **1.24V for CNVi logic**. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide for implementation details. |
| **VCCDPHY_EC_1P24** | For decoupling capacitor only. This rail should NOT be driven from the motherboard. This rail can optionally be connected to VCCDPHY_1P24 on the motherboard. |
| **VCCPHVLDO_1P8** | **1.8V Primary Well.** On the motherboard, this power pin must be connected to VCCPRIM_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode. |
| **VCCPGPPA** | **1.8V or 3.3V for GPP_A group.** |
| **VCCPGPPBC** | **1.8V or 3.3V for GPP_B and GPP_C groups.** |
| **VCCPGPPD** | **1.8V or 3.3V for GPP_D group.** |
| **VCCPGPPEF** | **1.8V or 3.3V for GPP_E and GPP_F groups.** |
| **VCCPGPPG_3P3** | **3.3V for GPP_G group.** |
| **VCCPGPPHK** | **1.8V or 3.3V for GPP_H and GPP_K groups.** |
| **VCCMPHY_SENSE** | **1.05V Sense Line.** |
| **VSSMPHY_SENSE** | **0V (Ground) Sense Line.** |
| **VSS** | **Ground.** |

https://vinafix.com

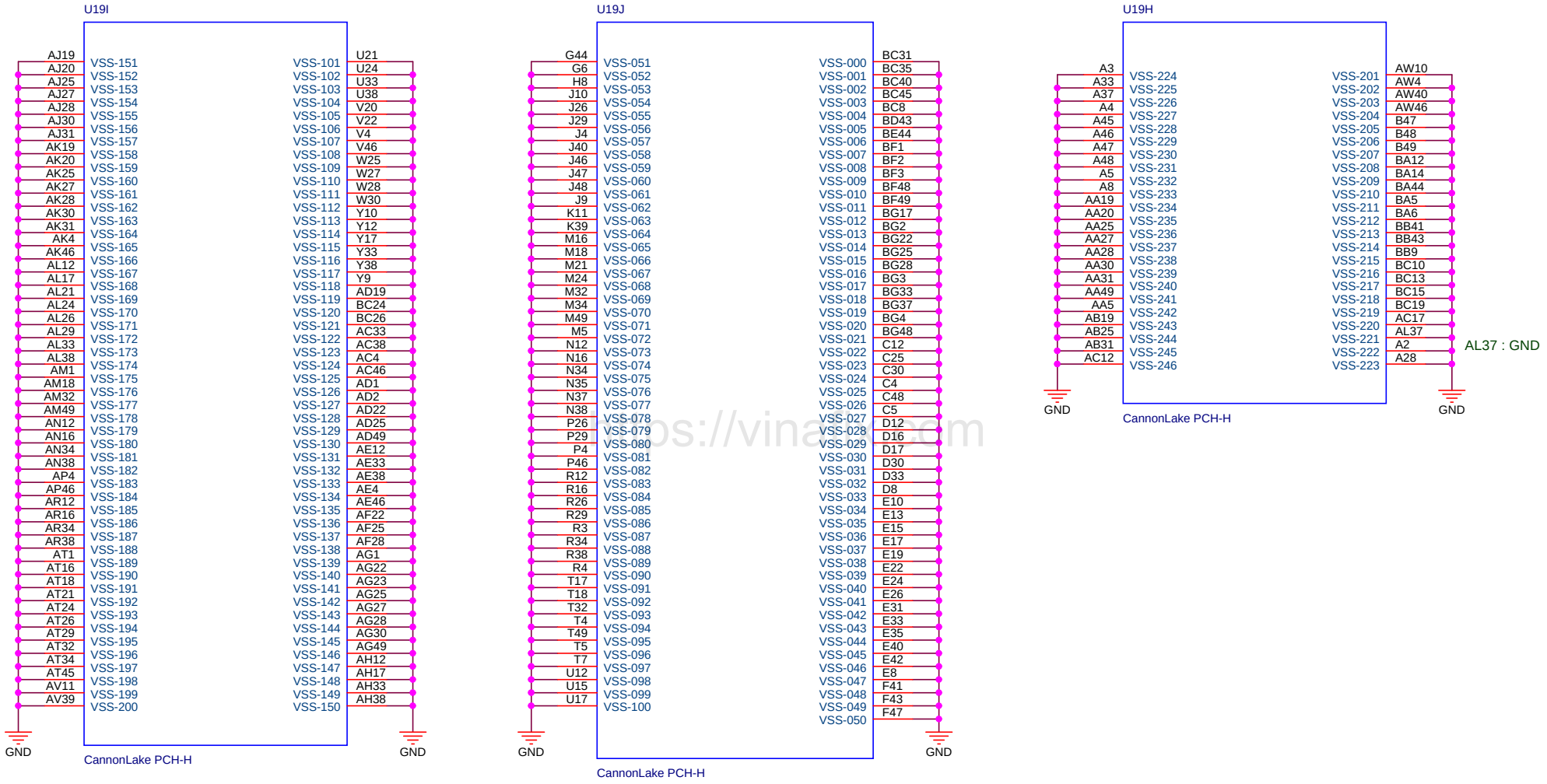
MICRO-STAR INT'L CO.,LTD.

Title: PCH-6(Power)

Size: Custom | Document Number: MS-16K51 | Rev: 0B

Date: Friday, October 13, 2017 | Sheet 38 of 80

# PCH-H(GND)

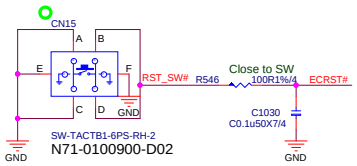



https://vinafix.com

| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | |
| Title: PCH-7(GND) | | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B |
| Date: Friday, October 06, 2017 | Sheet 39 of 80 | |

# KBC/EC/uP (ENE9028)

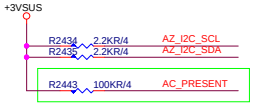
## Hardware Reset

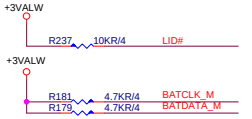


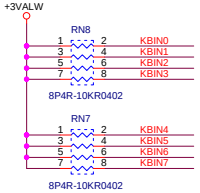

remove OVERT# (Active Low)

## PU/PD

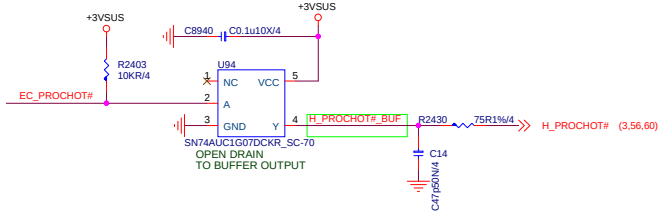
RSMRST# follow DG modify to 10K

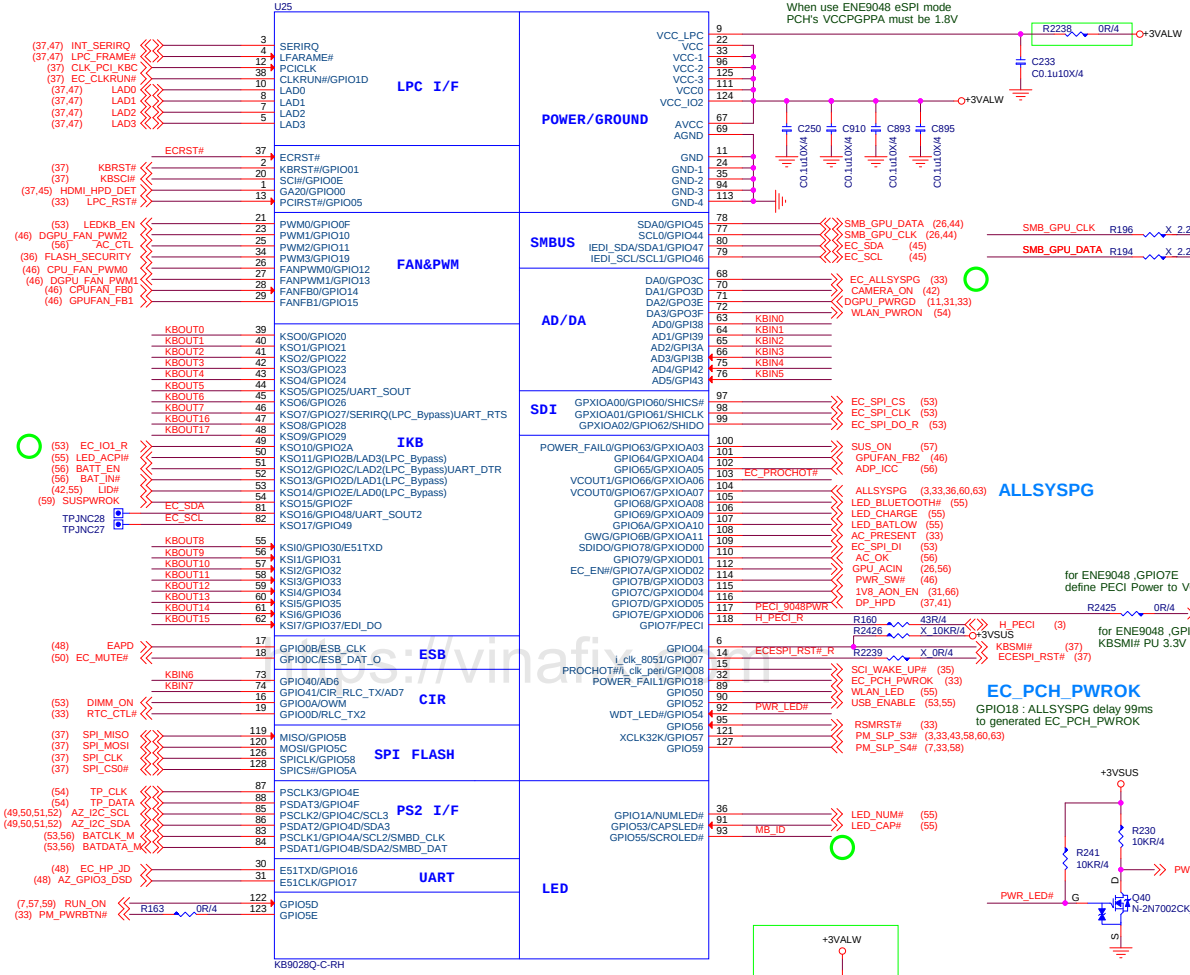


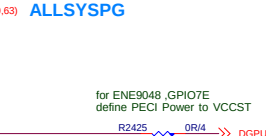




## EC_PROCHOT#




When use ENE9048 eSPI mode
PCH's VCCPGPPA must be 1.8V

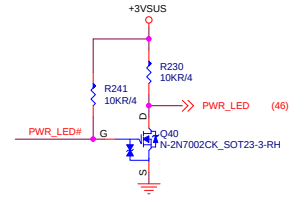


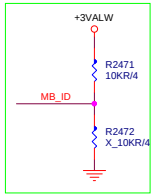

for ENE9048 ,GPIO7E
define PECI Power to VCCST

for ENE9048 ,GPIO04
KBSMI# PU 3.3V

## EC_PCH_PWROK

GPIO18 : ALLSYSPG delay 99ms
to generated EC_PCH_PWROK




## MB_ID

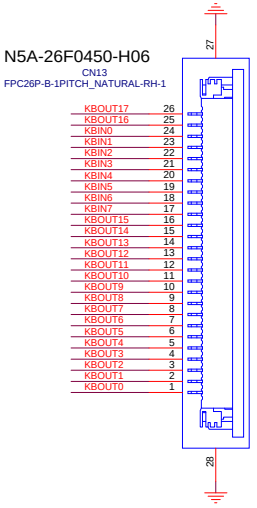
Pull High : per key of color KB
Pull Low : 3 Area of color KB

## ENE9028 & 9048 Power Notes :

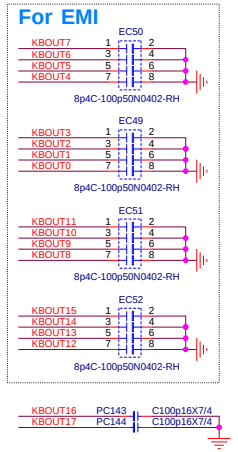
pin9 VCCLPC :
3.3V for ENE9028's LPC mode.
1.8V for ENE9048's eSPI mode.

pin111 VCC0 :
3.3V for ENE9028's PLC function
3.3V for ENE9048's eSPI operation with Pre-Driver.

## N5A-26F0450-H06




## For EMI







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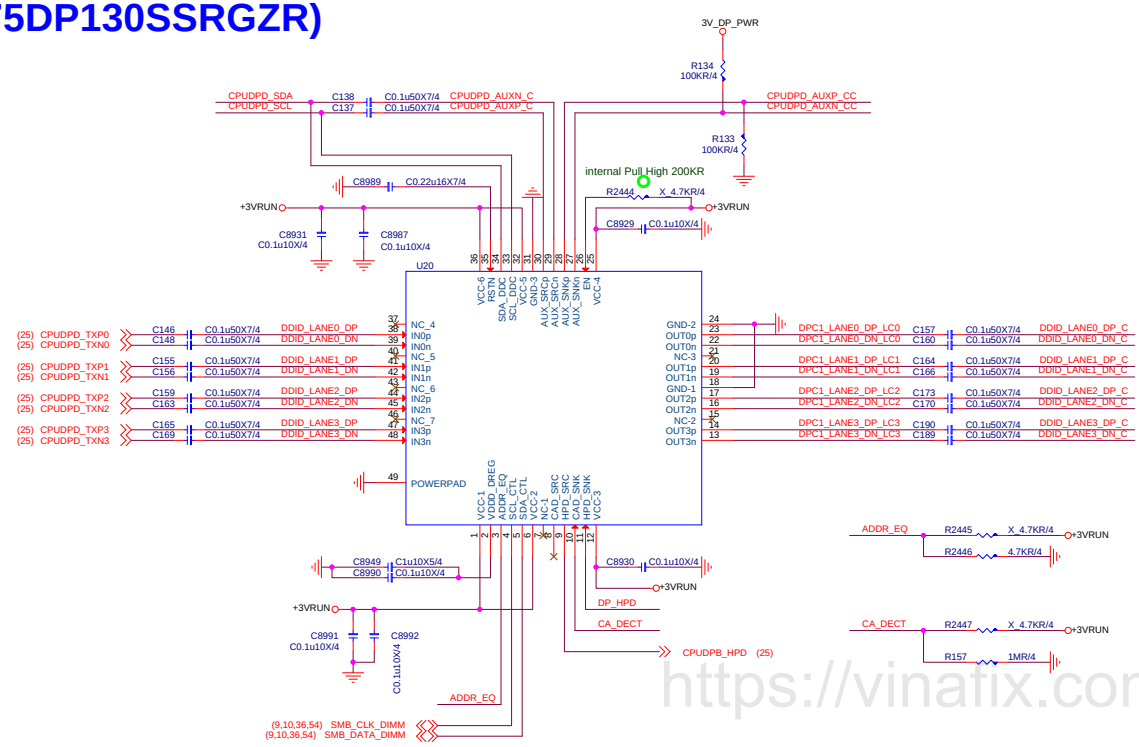
| | | | |
|---|---|---|---|
| msi | MICRO-STAR INT'L CO.,LTD. | | |
| Title | KBC/EC/uP (ENE9028) | | |
| Size: Custom | Document Number: MS-16K51 | | Rev: 0B |
| Date: Friday, October 13, 2017 | | Sheet 40 of 80 | |

# DP 1.2 Redriver (TI/SN75DP130SSRGZR)

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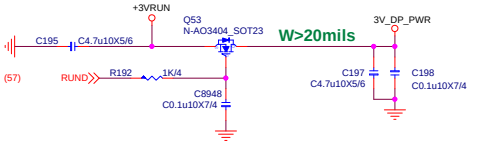
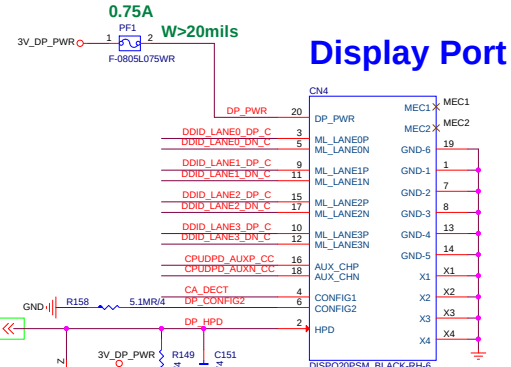
Avoid DP Leakage



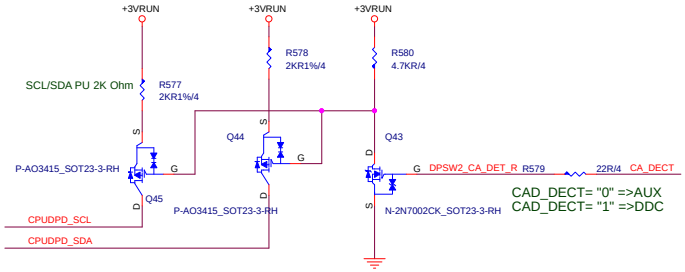



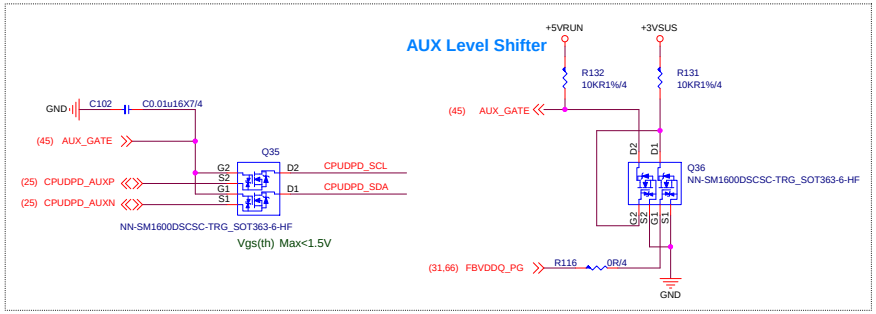

## Display Port

N5W-20M0500-H06

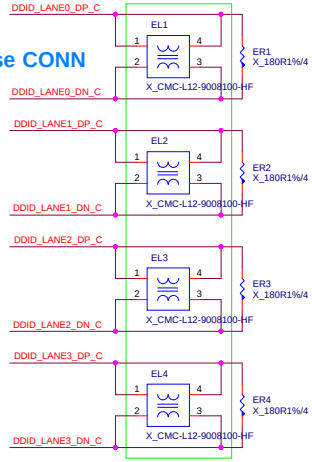
CAD_SNK Have internal Pull down 1Mohm.
HPD_SNK Have internal Pull down 150kohm.
No problem with Leakage from DP device
The DP_PWR and RETURN pins of the box-to-box connectors must support the maximum current rating of 500mA.

## For Dual Mode Switch to DDC




## EMI Close CONN



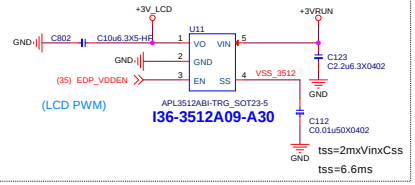

MICRO-STAR INT'L CO.,LTD.

| | | |
|---|---|---|
| Title | DP 1.4 (TUSB546-DCI) | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B |
| Date: Tuesday, October 17, 2017 | Sheet 41 of 80 | |

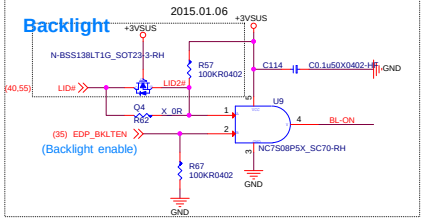
# eDP Connector

N5A-40F0180-A81

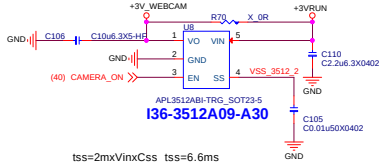
## Pannel Device Logic Power



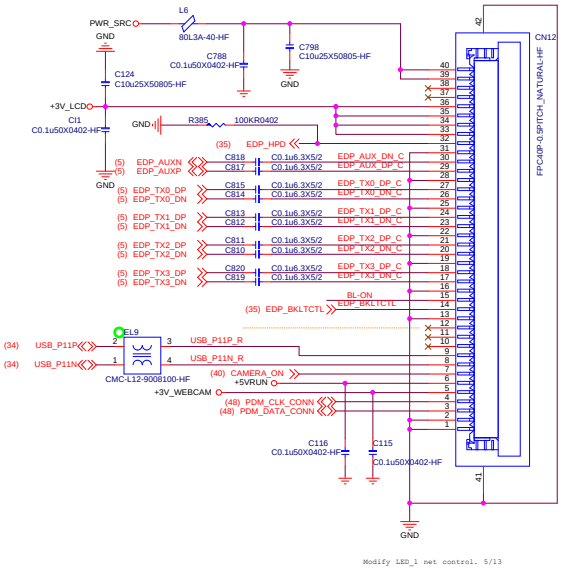

## Backlight

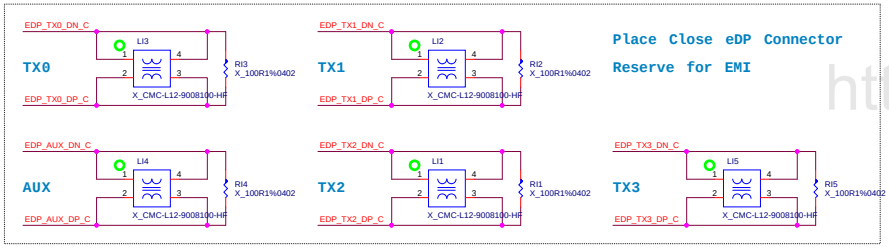



## CAMERA Power




## eDP CONN



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## LCD Module Pin Define FOR FULL HD PANEL

| Pin No | Symbol | Description |
|---|---|---|
| 1 | Vcom SDA | Vcom IIC SDA |
| 2 | H_GND | High Speed Ground |
| 3 | LAN1_N | Complement Signal-Lane 1 |
| 4 | LAN1_P | True Signal-Main Lane 1 |
| 5 | H_GND | High Speed Ground |
| 6 | LAN0_N | Complement Signal-Lane 0 |
| 7 | LAN0_P | True Signal-Main Lane 0 |
| 8 | H_GND | High Speed Ground |
| 9 | AUX+ | True Signal-Auxiliary Channel |
| 10 | AUX- | Complement Signal-Auxiliary Channel |
| 11 | H_GND | High Speed Ground |
| 12 | LCD_VCC | Power Supply +3.3 V (typical) |
| 13 | LCD_VCC | Power Supply +3.3 V (typical) |
| 14 | NC | No Connection (Reserved for CMI test) |
| 15 | H_GND | Ground |
| 16 | H_GND | Ground |
| 17 | HPD | Hot Plug Detect |
| 18 | BL_GND | BL Ground |
| 19 | BL_GND | BL Ground |
| 20 | BL_GND | BL Ground |
| 21 | BL_GND | BL Ground |
| 22 | BL_EN | BL_Enable Signal of LED Converter |
| 23 | BL_PWM | PWM Dimming Control Signal of LED Converter |
| 24 | Vcom SCL | Vcom IIC SCL |
| 25 | NC | No Connection (Reserved) |
| 26 | LED_VCCS | BL Power |
| 27 | LED_VCCS | BL Power |
| 28 | LED_VCCS | BL Power |
| 29 | LED_VCCS | BL Power |
| 30 | NC | No Connection (Reserved) |

## LCD Module Pin Define FOR WQHD PANEL

| Pin No | Symbol | Description |
|---|---|---|
| 1 | NC | Reserved for LCD manufactureer's use |
| 2 | H_GND | High Speed Ground |
| 3 | Lane3_N | Complement Signal Link Lane 3 |
| 4 | Lane3_P | True Signal Link Lane 3 |
| 5 | H_GND | High Speed Ground |
| 6 | Lane2_N | Complement Signal Link Lane 2 |
| 7 | Lane2_P | True Signal Link Lane 2 |
| 8 | H_GND | High Speed Ground |
| 9 | Lane1_N | Complement Signal Link Lane 1 |
| 10 | Lane1_P | True Signal Link Lane 1 |
| 11 | H_GND | High Speed Ground |
| 12 | Lane0_N | Complement Signal Link Lane 0 |
| 13 | Lane0_P | True Signal Link Lane 0 |
| 14 | H_GND | High Speed Ground |
| 15 | AUX_CH_P | True Signal Auxiliary Channel |
| 16 | AUX_CH_N | Complement Signal Auxiliary Channel |
| 17 | H_GND | High Speed Ground |
| 18 | VDD | LCD logic and driver power(3.3V) |
| 19 | VDD | LCD logic and driver power(3.3V) |
| 20 | VDD | LCD logic and driver power(3.3V) |
| 21 | VDD | LCD logic and driver power(3.3V) |
| 22 | BIST | BIST patterns selection<br>L : Disable [default] , H : Enable |
| 23 | LCD_GND | LCD logic and driver ground |
| 24 | LCD_GND | LCD logic and driver ground |
| 25 | LCD_GND | LCD logic and driver ground |
| 26 | LCD_GND | LCD logic and driver ground |
| 27 | HPD | HPD signal pin |
| 28 | BL_GND | Backlight ground |
| 29 | BL_GND | Backlight ground |
| 30 | BL_GND | Backlight ground |
| 31 | BL_GND | Backlight ground |
| 32 | BL_ENABLE | Backlight On/Off |
| 33 | BL_PWM_DIM | System PWM |
| 34 | NC | Reserved for LCD manufacturer's use |
| 35 | NC | Reserved for LCD manufacturer's use |
| 36 | VBL | Backlight power |
| 37 | VBL | Backlight power |
| 38 | VBL | Backlight power |
| 39 | VBL | Backlight power |
| 40 | NC | No Connection (Reserved) |

## LCD Module Pin Define FOR QHD+ PANEL

| Pin No | Symbol | Description |
|---|---|---|
| 1 | NC | Reserved for LCD manufacturer' s use |
| 2 | H_GND | High Speed Ground |
| 3 | Lane3_N | Complement Signal Link Lane 3 |
| 4 | Lane3_P | True Signal Link Lane 3 |
| 5 | H_GND | High Speed Ground |
| 6 | Lane2_N | Complement Signal Link Lane 2 |
| 7 | Lane2_P | True Signal Link Lane 2 |
| 8 | H_GND | High Speed Ground |
| 9 | Lane1_N | Complement Signal Link Lane 1 |
| 10 | Lane1_P | True Signal Link Lane 1 |
| 11 | H_GND | High Speed Ground |
| 12 | Lane0_N | Complement Signal Link Lane 0 |
| 13 | Lane0_P | True Signal Link Lane 0 |
| 14 | H_GND | High Speed Ground |
| 15 | AUX_CH_P | True Signal Auxiliary Channel |
| 16 | AUX_CH_N | Complement Signal Auxiliary Channel |
| 17 | H_GND | High Speed Ground |
| 18 | NC | Reserved for LCD manufacturer' s use |
| 19 | NC | Reserved for LCD manufacturer' s use |
| 20 | VDD | LCD logic and driver power(3.3V) |
| 21 | VDD | LCD logic and driver power(3.3V) |
| 22 | VDD | LCD logic and driver power(3.3V) |
| 23 | VDD | LCD logic and driver power(3.3V) |
| 24 | VDD | LCD logic and driver power(3.3V) |
| 25 | NC | Reserved for LCD manufacturer' s use |
| 26 | LCD_GND | LCD logic and driver ground |
| 27 | LCD_GND | LCD logic and driver ground |
| 28 | LCD_GND | LCD logic and driver ground |
| 29 | LCD_GND | LCD logic and driver ground |
| 30 | LCD_GND | LCD logic and driver ground |
| 31 | HPD | Backlight ground |
| 32 | NC | Reserved for LCD manufacturer' s use |
| 33 | PWM_OUT | PWM_OUT |
| 34 | PWM_IN | PWM_IN |
| 35 | NC | Reserved for LCD manufacturer' s use |
| 36 | NC | Reserved for LCD manufacturer' s use |
| 37 | NC | Reserved for LCD manufacturer' s use |
| 38 | VBL | LED Anode |
| 39 | VBL | LED Anode |
| 40 | NC | Reserved for LCD manufacturer' s use |
| 41 | LED_C1 | LED Cathode 1 |
| 42 | LED_C2 | LED Cathode 2 |
| 43 | LED_C3 | LED Cathode 3 |
| 44 | LED_C4 | LED Cathode 4 |
| 45 | LED_C5 | LED Cathode 5 |
| 46 | LED_C6 | LED Cathode 6 |
| 47 | LED_C7 | LED Cathode 7 |
| 48 | LED_C8 | LED Cathode 8 |
| 49 | NC | Reserved for LCD manufacturer' s use |
| 50 | NC | Reserved for LCD manufacturer' s use |

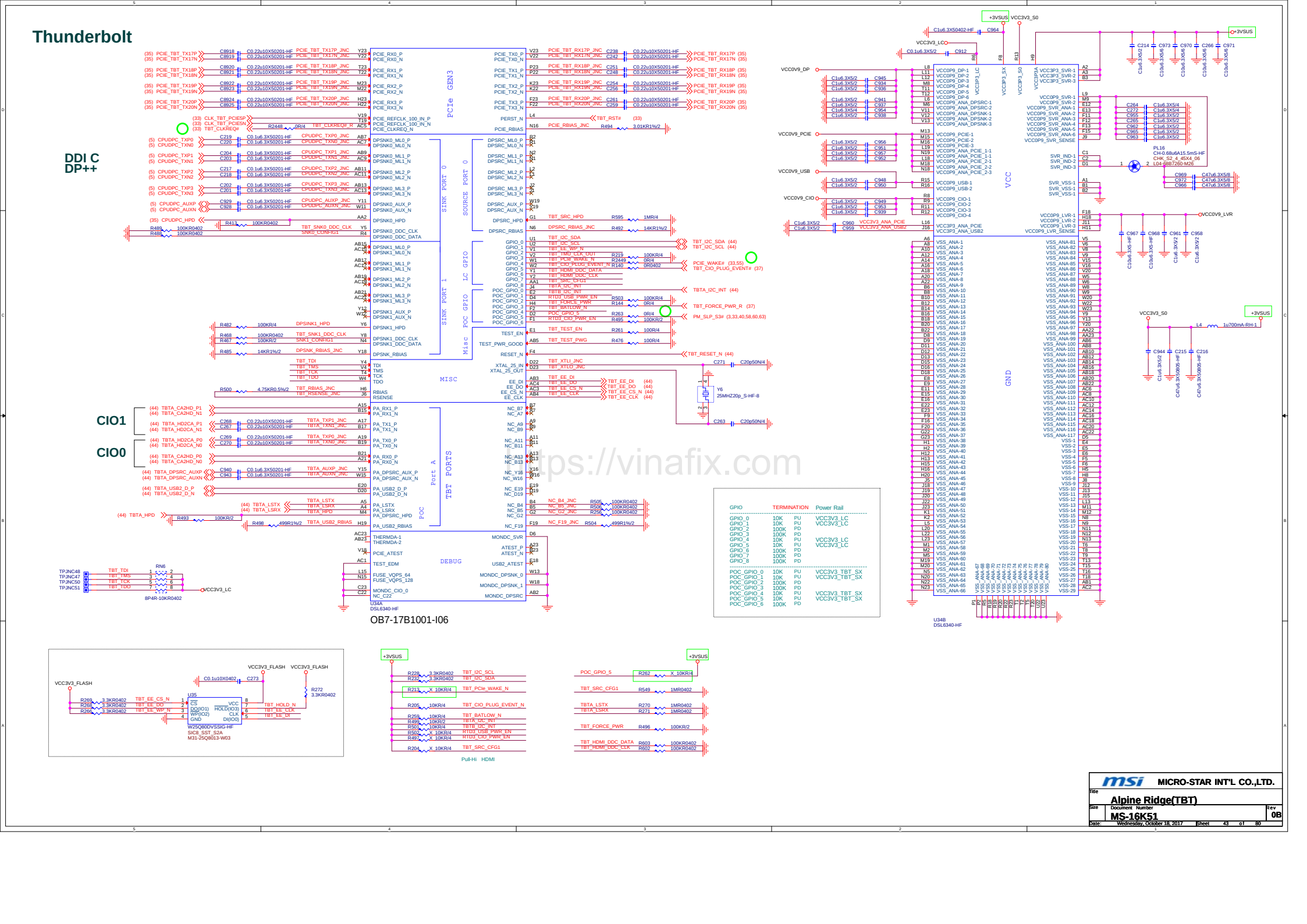
MICRO-STAR INT'L CO.,LTD.

Title: eDP Connector/Camera

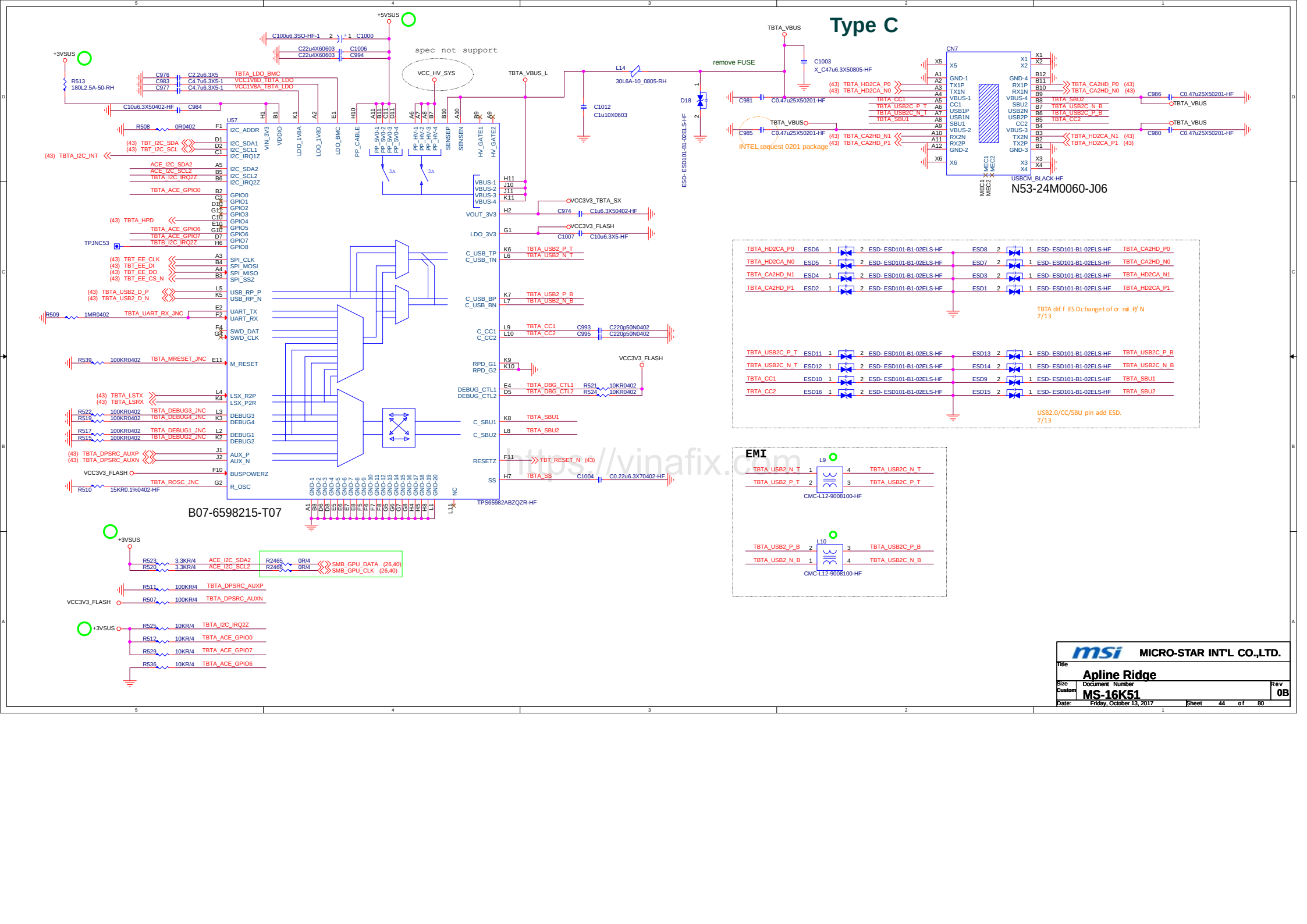
Size: Custom | Document Number: MS-16K51 | Rev: 0B

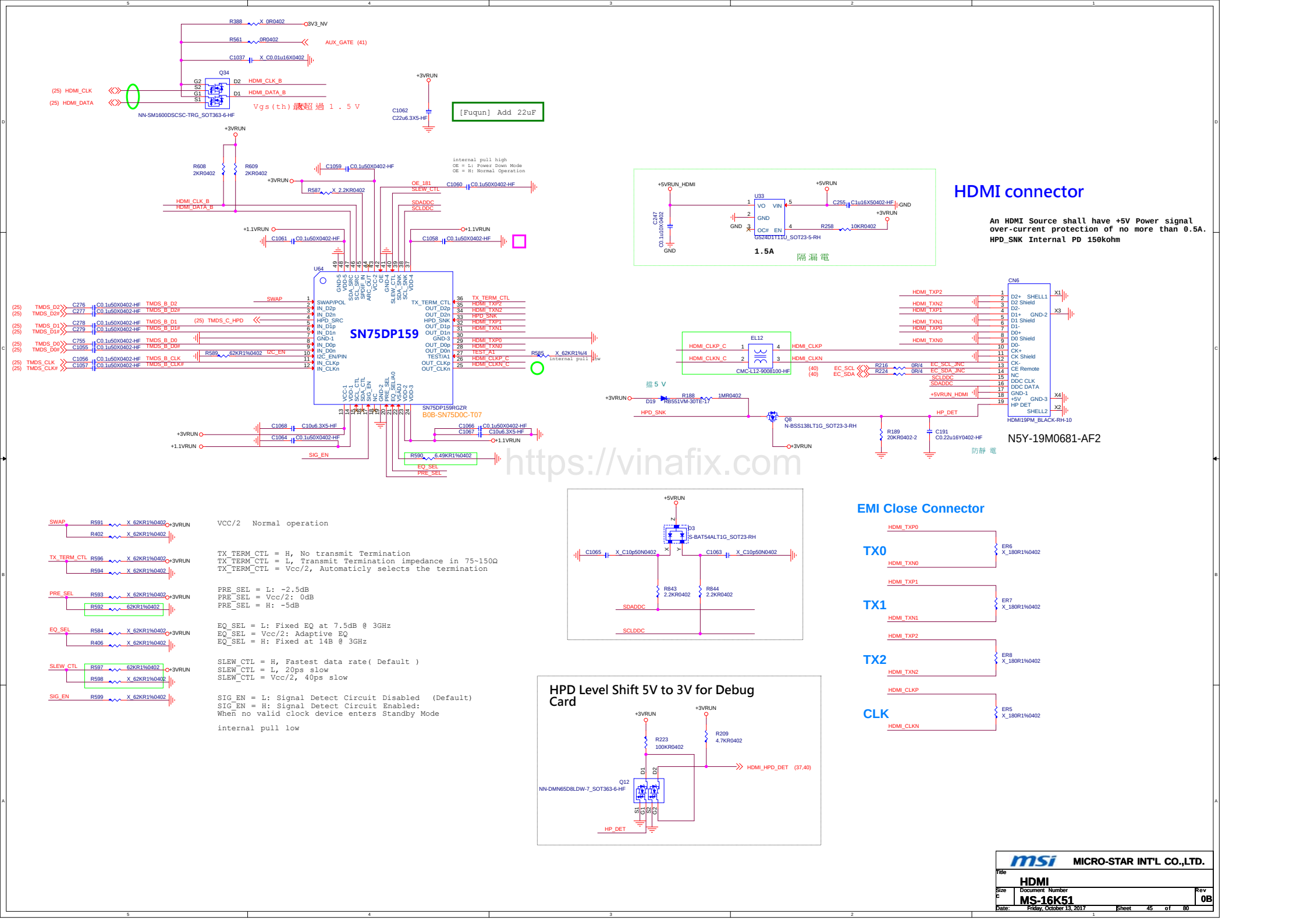
Date: Friday, October 06, 2017 | Sheet 42 of 80

# Thunderbolt



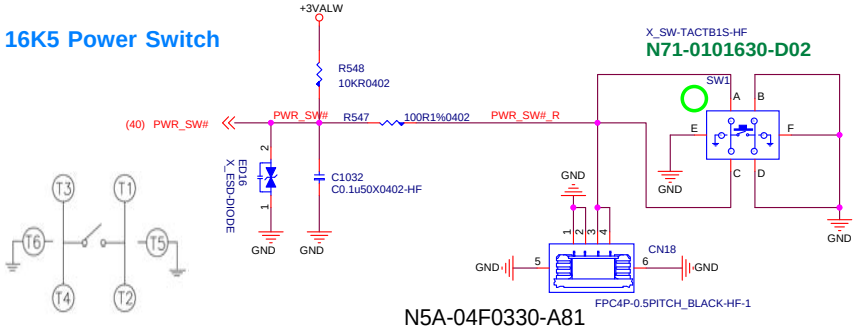

| | | | |
|---|---|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD. | | |
| Title | Alpine Ridge(TBT) | | |
| Size | Document Number MS-16K51 | | Rev 0B |
| Date: | Wednesday, October 18, 2017 | Sheet 43 of 80 | |


Type C
spec not support
VCC_HV_SYS
TBTA_VBUS_L
remove FUSE
INTEL request 0201 package
N53-24M0060-J06
B07-6598215-T07
TPS65982ABZQZR-HF
USBCM_BLACK-HF
CMC-L12-9008100-HF
EMI
TBTA diff ESD change to orm P/N 7/13
USB2.0/CC/SBU pin add ESD. 7/13
https://vinafix.com
MICRO-STAR INT'L CO.,LTD.
Apline Ridge
MS-16K51
0B
Friday, October 13, 2017
Sheet 44 of 80


HDMI connector
An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.
HPD_SNK Internal PD 150kohm
SN75DP159
SN75DP159RGZR
B0B-SN75D0C-T07
N5Y-19M0681-AF2
HDMI19PM_BLACK-RH-10
CMC-L12-9008100-HF
G524D1T11U_SOT23-5-RH
1.5A
隔漏電
防靜電
EMI Close Connector
TX0
TX1
TX2
CLK
HPD Level Shift 5V to 3V for Debug Card
NN-SM1600DSCSC-TRG_SOT363-6-HF
NN-DMN65D8LDW-7_SOT363-6-HF
S-BAT54ALT1G_SOT23-RH
N-BSS138LT1G_SOT23-3-RH
RB551VM-30TE-17
[Fuqun] Add 22uF
Vgs(th)最超過 1.5V
VCC/2 Normal operation
TX_TERM_CTL = H, No transmit Termination
TX_TERM_CTL = L, Transmit Termination impedance in 75~150Ω
TX_TERM_CTL = Vcc/2, Automaticly selects the termination
PRE_SEL = L: -2.5dB
PRE_SEL = Vcc/2: 0dB
PRE_SEL = H: -5dB
EQ_SEL = L: Fixed EQ at 7.5dB @ 3GHz
EQ_SEL = Vcc/2: Adaptive EQ
EQ_SEL = H: Fixed at 14B @ 3GHz
SLEW_CTL = H, Fastest data rate( Default )
SLEW_CTL = L, 20ps slow
SLEW_CTL = Vcc/2, 40ps slow
SIG_EN = L: Signal Detect Circuit Disabled (Default)
SIG_EN = H: Signal Detect Circuit Enabled:
When no valid clock device enters Standby Mode
internal pull low
internal pull high
OE = L: Power Down Mode
OE = H: Normal Operation
https://vinafix.com
MICRO-STAR INT'L CO.,LTD.
Title
HDMI
Size C
Document Number
MS-16K51
Rev 0B
Date: Friday, October 13, 2017
Sheet 45 of 80

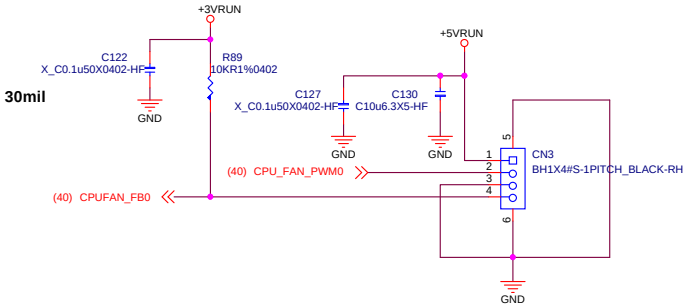
# PWR SW/CPU FAN/BTB CONN/ LED CONN

## 16K5 Power Switch



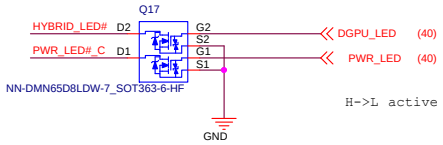

N5A-04F0330-A81

## CPU FAN

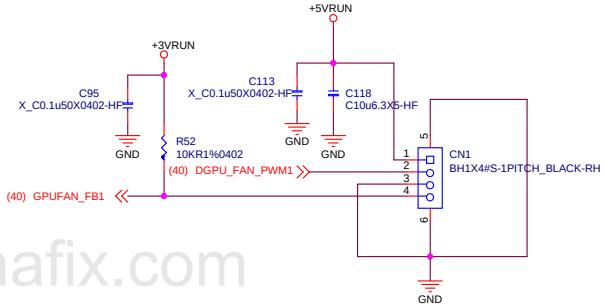



## Control PWR LED

| DGPU_LED | PWR_LED | LED COLOR |
|---|---|---|
| L | H | RED |
| H | H | ORANGE |
| H | L | GREEN |
| L | L | X |



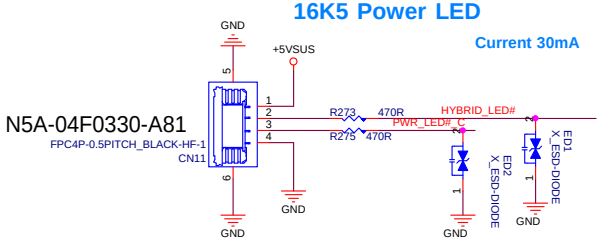

## DGPU FAN

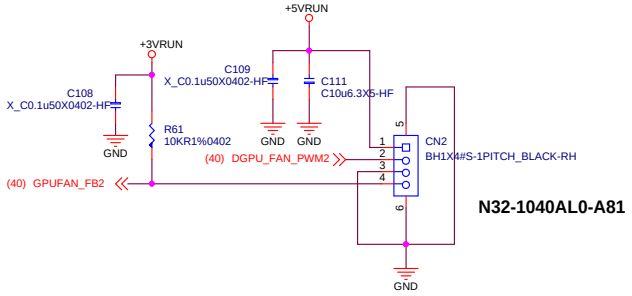



https://vinafix.com

## 16K5 Power LED

Current 30mA



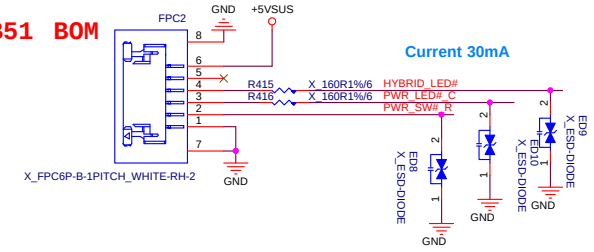




N32-1040AL0-A81

## Power LED+SW

**17B51 BOM**

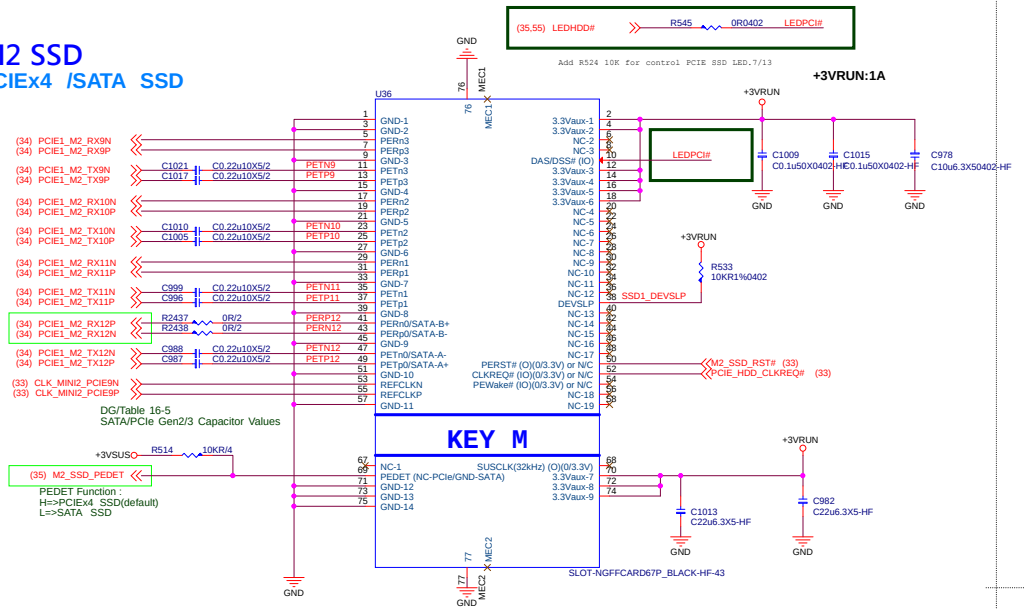
Current 30mA




| | | |
|---|---|---|
| msi | MICRO-STAR INT'L CO.,LTD. | |
| Title | CPU FAN/BTB CONN/LED | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B |
| Date: Thursday, October 05, 2017 | Sheet 46 of 80 | |

# M2 SSD

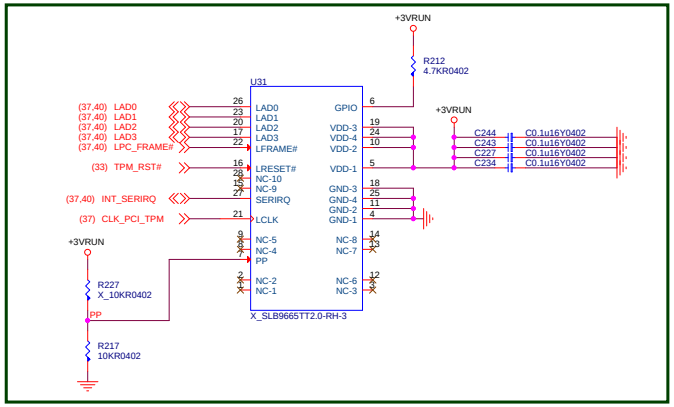
## PCIEx4 /SATA SSD




N15-0670530-L41

| | | |
|---|---|---|
| 40 | NC | No Connect |
| 41 | SATA-B+/PERn0 | Host receiver differential signal pair |
| 42 | NC | No Connect |
| 43 | SATA-B-/PERp0 | Host receiver differential signal pair |
| 44 | NC | No Connect |
| 45 | GND | Ground |
| 46 | NC | No Connect |
| 47 | SATA-A-/PETn0 | Host Transmitter differential signal pair |
| 48 | NC | No Connect |
| 49 | SATA-A+/PETp0 | Host transmitter differential signal pair |

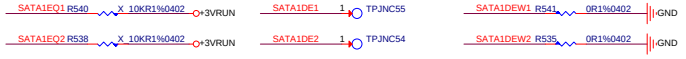
# TPM




Physical Presence(PP)
The standard position of the jumper should connect the pin to GND. If the pin is connected to VDD, some special commands are enabled .

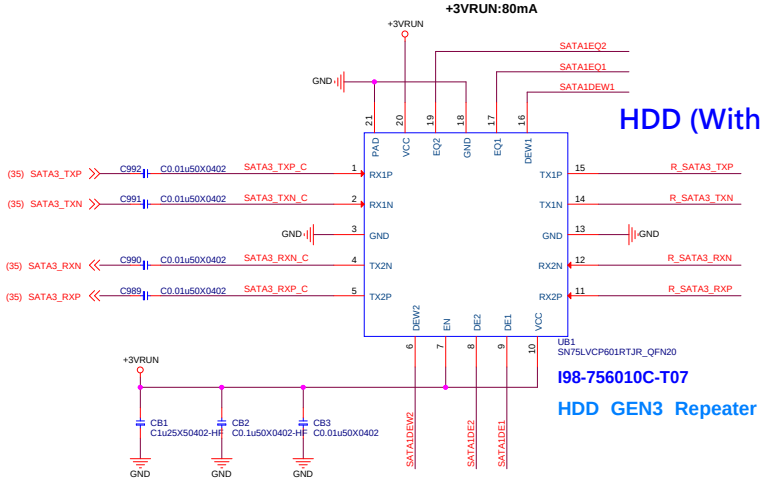
| DE1/DE2 | CH1/CH2De-Emphasis dB (at 6Gbps) | EQ1/EQ2 | CH1/CH2Equalization dB (at 6Gbps) |
|---|---|---|---|
| NC (*default*) | –4 | NC (*default*) | 0 |
| 0 | 0 | 0 | 7 |
| 1 | –2 | 1 | 14 |

| DEW1/DEW2 | Device Function → DE Width for CH1/CH2 |
|---|---|
| 0 | De-emphasis pulse duration, short (recommended setting when link operates at SATA 1.5/3/6 Gbps) |
| 1 (*default*) | De-emphasis pulse duration, long (recommended setting when link operates at SATA 1.5/3 Gbps speed only) |




TI SN75LVCP601RTJR HW Setting

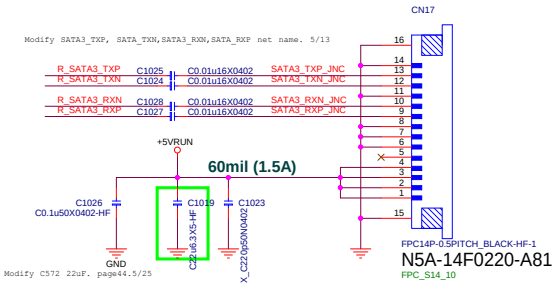
# HDD (With Repeater)




I98-756010C-T07

HDD GEN3 Repeater

# HDD2




(Must used the gold fresh type)

MICRO-STAR INT'L CO.,LTD.

Title: M2 SSD/HDD/TPM

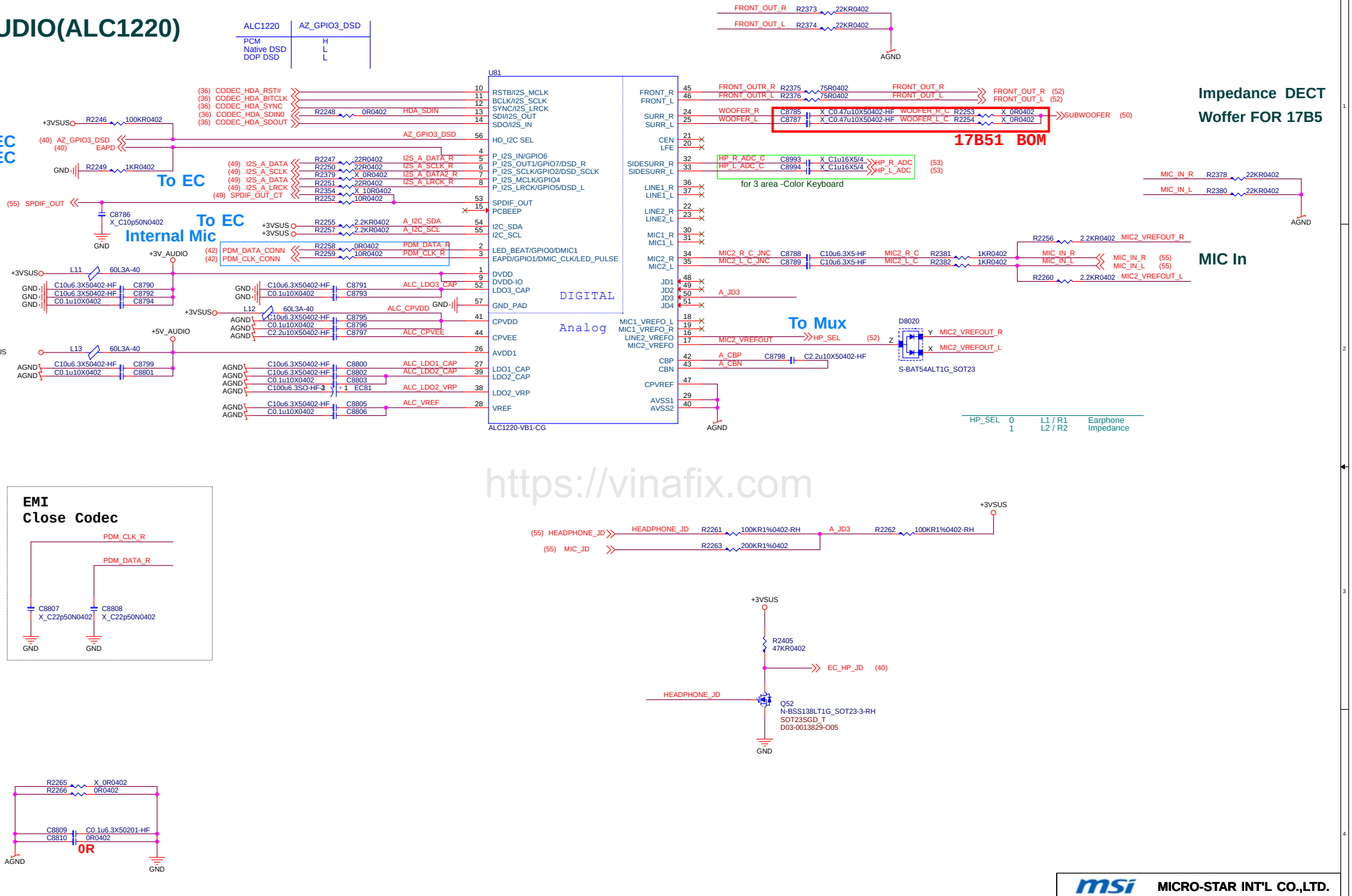
Size: Custom | Document Number: MS-16K51 | Rev: 0B

Date: Thursday, October 05, 2017 | Sheet 47 of 80

https://vinafix.com

# AUDIO(ALC1220)

| ALC1220 | AZ_GPIO3_DSD |
|---|---|
| PCM | H |
| Native DSD | L |
| DOP DSD | L |




https://vinafix.com

## EMI Close Codec







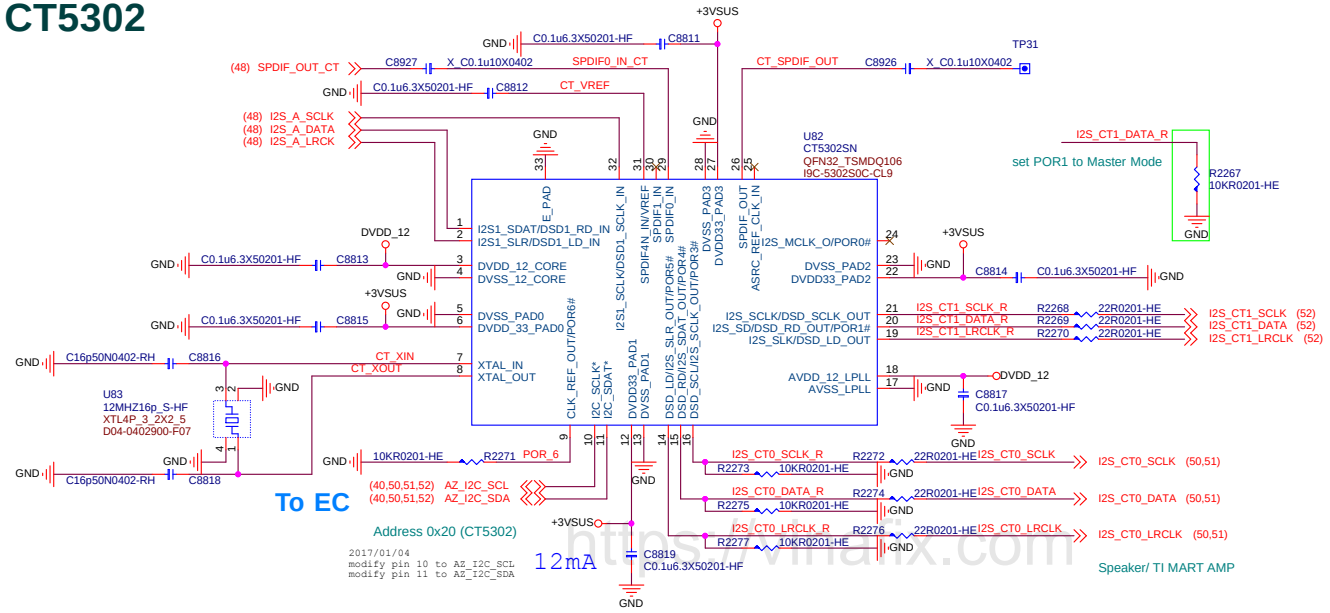


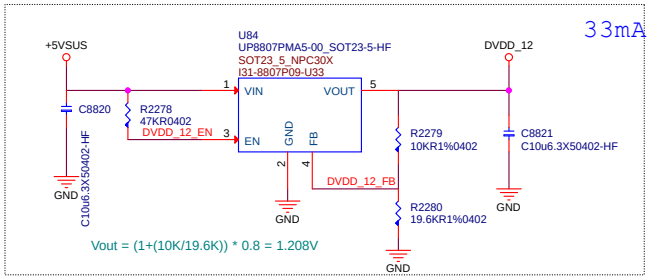




| | | | |
|---|---|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD. | | |
| Title | Audio(ALC1220) | | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B | |
| Date: Wednesday, October 18, 2017 | Sheet 48 of 80 | | |

# CT5302




HW SETTING

**I2S output slave mode:**

Select I2S1 output port

| No. | POR1 | Definition |
|---|---|---|
| 0 | 0 | I2S output master mode |
| 1 | 1 | I2S output slave mode |

HW SETTING

**Hardware Crystal:**

Select current external crystal frequency

| No | POR4 | POR3 | Definition |
|---|---|---|---|
| 0 | 0 | 0 | 12.0000MHz |
| 1 | 0 | 1 | 11.2896MHz |
| 2 | 1 | 0 | 12.2880MHz |
| 3 | 1 | 1 | 14.3180MHz |

HW SETTING

**I2C Slave ID**

Define chip I2C slave address

| No | POR6 | POR5 | Definition |
|---|---|---|---|
| 0 | 0 | 0 | 0x20 |
| 1 | 0 | 1 | 0x22 |
| 2 | 1 | 0 | 0x24 |
| 3 | 1 | 1 | 0x26 |

| Pin Name | Description | Function Table |
|---|---|---|
| POR_IN_1 | POWER_ON_LATCH_DC[1] = SEL_I2S_TX_SLAVE_MODE | Select I2S1 output port is master or slave mode |
| POR_IN_3 | POWER_ON_LATCH_DC[4:3] = SEL_XTAL[1:0] | Select Crystal frequency |
| POR_IN_4 | | |
| POR_IN_5 | POWER_ON_LATCH_DC[6:5] = I2C_ID[1:0] | I2C serial interface device ID selection |
| POR_IN_6 | | |

MICRO-STAR INT'L CO.,LTD.

Title: CT5302

Size: Custom | Document Number: MS-16K51 | Rev: 0B

Date: Thursday, October 05, 2017 | Sheet 49 of 80

https://vinafix.com

# SMART AMP LEFT

WIDTH > 40 mils

1.5A

PVCC=5V  Vpp=5*2=10.  Vrms=10/2.828=3.53
(RL=4 ohm) Po max =(Vrms) ^2/RL=(3.53)^2/4= 3.1W
I max=0.62 A

PVCC=19V  Vpp=19*2=38.  Vrms=38/2.828=13.43
(RL=4 ohm) Po max =(Vrms) ^2/RL=(13.43)^2/4= 45W
I max=2.3 A

To EC

2017/01/04
modify pin 36 to AZ_I2C_SCL
modify pin 35 to AZ_I2C_SDA

U85

TAS5766MRMTR_VQFN48-HF
VQFN48_T142X220
I71-5766M0C-T07

Address 0x98 (SPEAKER)

14dB/353-384KHz

# AMP WOOFER

## SPK L2 / Woffer FOR 17B5

17B51 BOM

YG Normal:3W,Max:3.5W 4ohm
10DB / 2W

4R/ 2W

APA3010XA-TRL_MSOP8-LF
I71-0301002-A30

H :Shutdown >2.2V
L: Active <0.4V

F(Low-pass) = 1/ 2π RC=1/(2π *3.3n*39K)=1.237k Hz

https://vinafix.com

# Left SPK+Woofer Conn

BH1X6#S-1.25PITCH_BLACK-RH
N32-1060720-A81

17B51 BOM

From EC

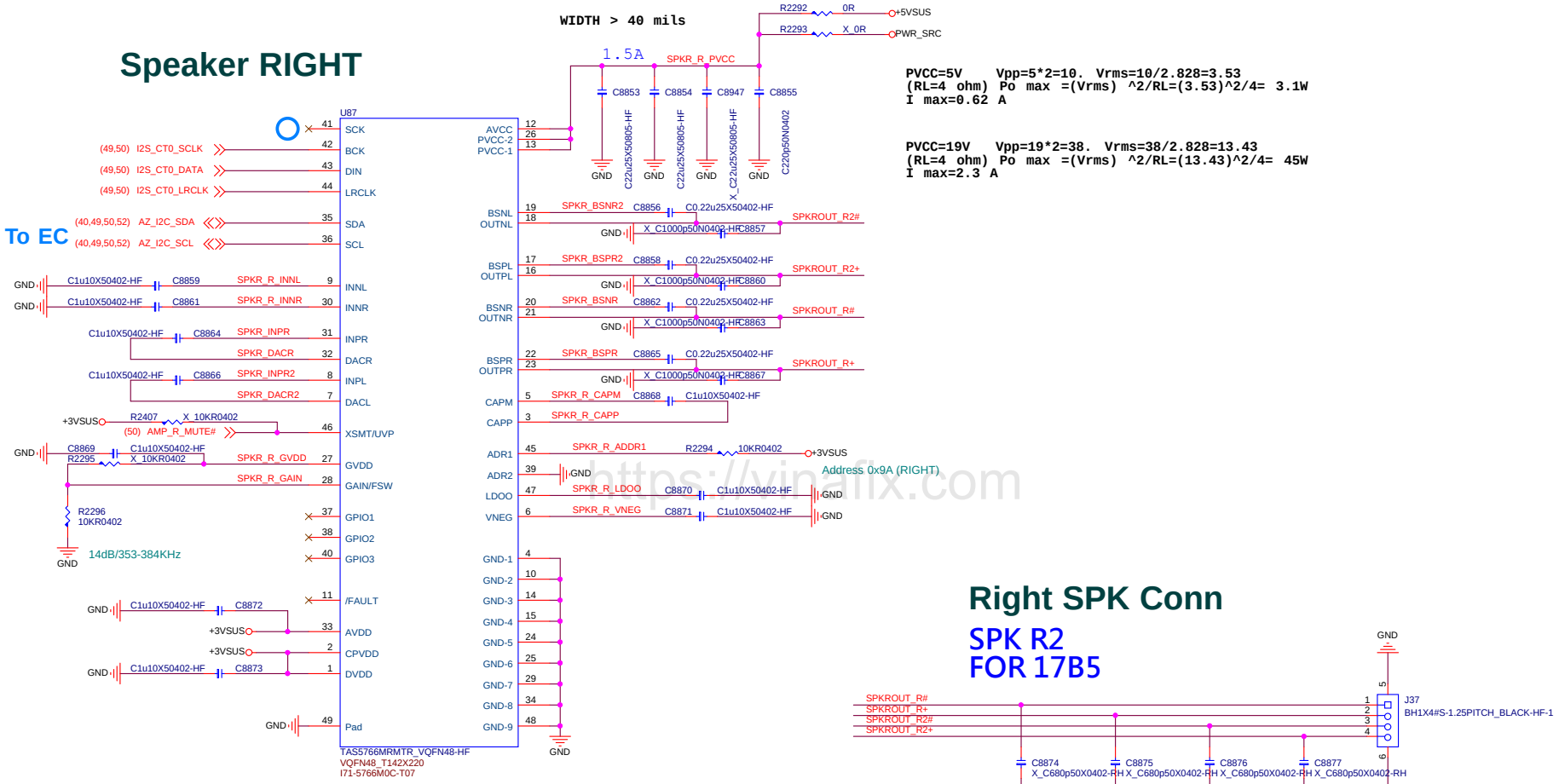
To WOOFER AMP

To SPEAK AMP

NN-DMN65D8LDW-7_SOT363-6-HF

| | |
|---|---|
| MICRO-STAR INT'L CO.,LTD. | |
| Title | SMART AMP L & WOOFER |
| Size: Custom | Document Number: MS-16K51 |
| Rev | 0B |
| Date: Thursday, October 05, 2017 | Sheet 50 of 80 |

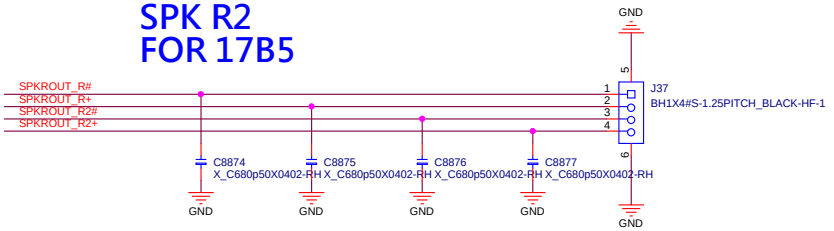
# Speaker RIGHT



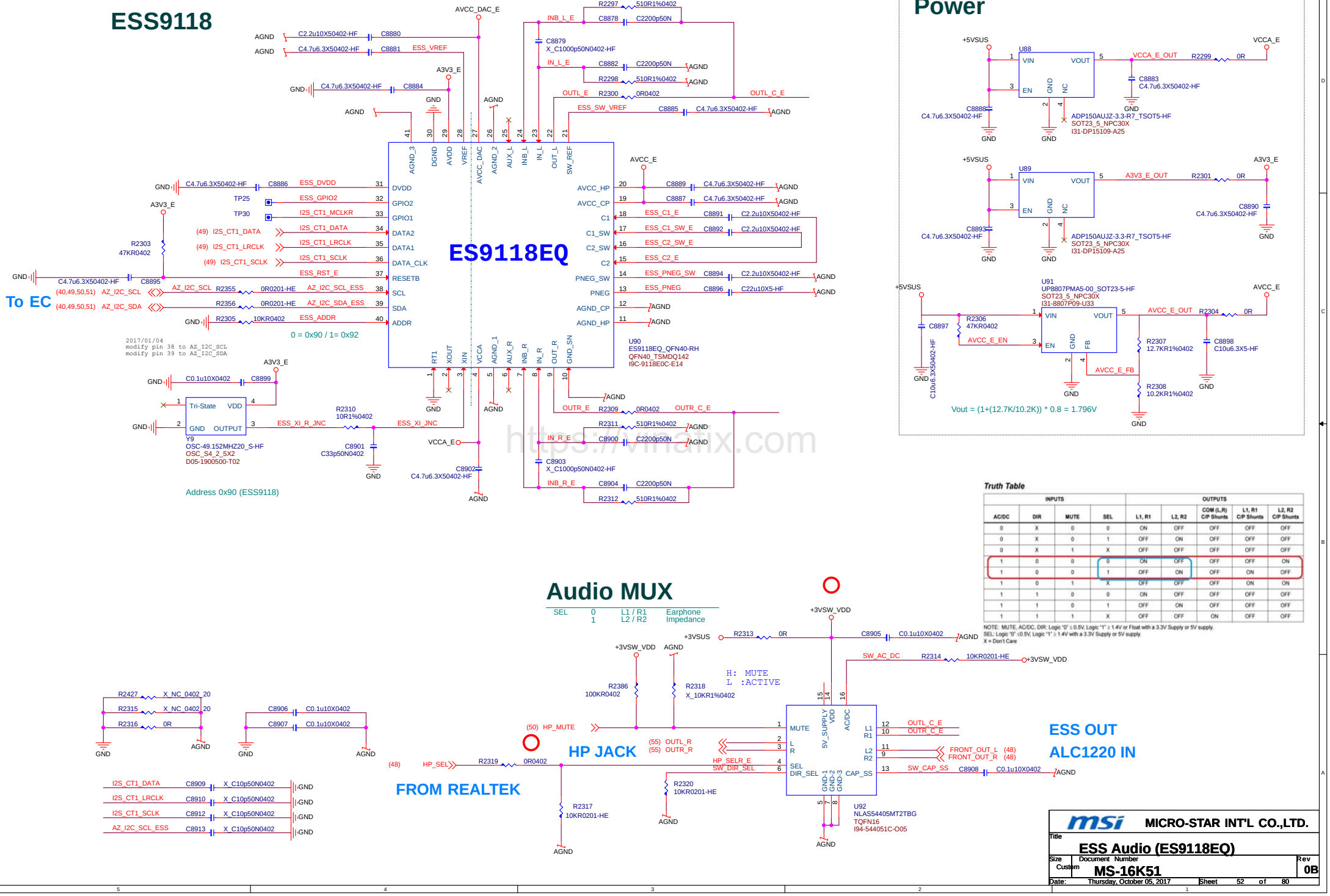

https://vinafix.com

# Right SPK Conn

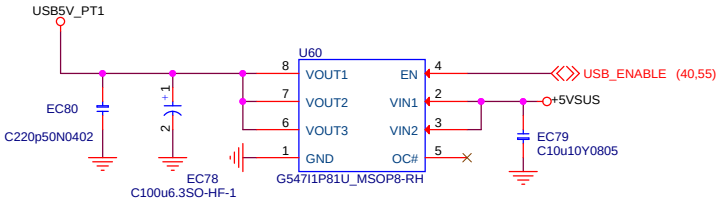
## SPK R2
## FOR 17B5




| | | | |
|---|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | | |
| Title: SMART AMP R | | | |
| Size: Custom | Document Number: MS-16K51 | | Rev: 0B |
| Date: Thursday, October 05, 2017 | | Sheet 51 of 80 | |

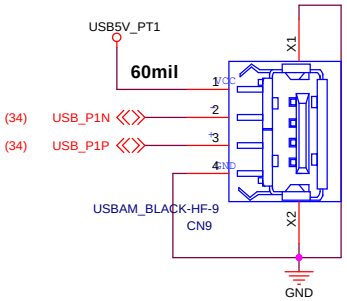

ESS9118
ES9118EQ
To EC
Address 0x90 (ESS9118)
0 = 0x90 / 1= 0x92
U90
ES9118EQ_QFN40-RH
QFN40_TSMDQ142
I9C-9118E0C-E14
Power
U88
U89
U91
ADP150AUJZ-3.3-R7_TSOT5-HF
SOT23_5_NPC30X
I31-DP15109-A25
UP8807PMA5-00_SOT23-5-HF
SOT23_5_NPC30X
I31-8807P09-U33
Vout = (1+(12.7K/10.2K)) * 0.8 = 1.796V
Audio MUX
SEL 0 L1 / R1 Earphone
1 L2 / R2 Impedance
H: MUTE
L :ACTIVE
HP JACK
FROM REALTEK
ESS OUT
ALC1220 IN
U92
NLAS54405MT2TBG
TQFN16
I94-544051C-O05
Truth Table
INPUTS
OUTPUTS
AC/DC
DIR
MUTE
SEL
L1, R1
L2, R2
COM (L,R) C/P Shunts
L1, R1 C/P Shunts
L2, R2 C/P Shunts
NOTE: MUTE, AC/DC, DIR: Logic "0" ≤ 0.5V, Logic "1" ≥ 1.4V or Float with a 3.3V Supply or 5V supply.
SEL: Logic "0" ≤0.5V, Logic "1" ≥ 1.4V with a 3.3V Supply or 5V supply.
X = Don't Care
MICRO-STAR INT'L CO.,LTD.
Title
ESS Audio (ES9118EQ)
Size
Custom
Document Number
MS-16K51
Rev
0B
Date: Thursday, October 05, 2017
Sheet 52 of 80

# USB2.0 CONN



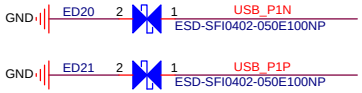

I36-5478102-G07

**G5478I1 MAX :2.5A**

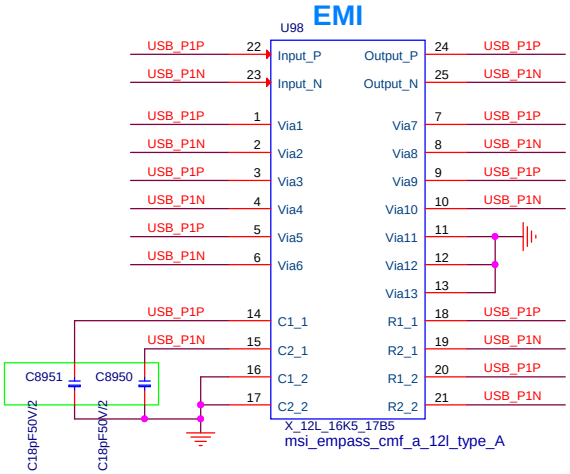



N53-04M1331-AF2

## ESD




## EMI



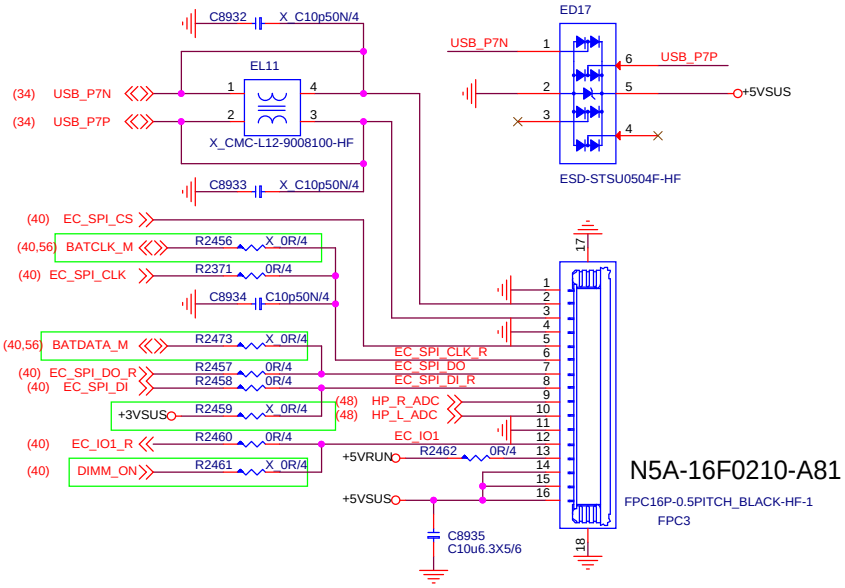

# SSE RGB Color Keyboard Control

https://vinafix.com

**16K51 BOM**

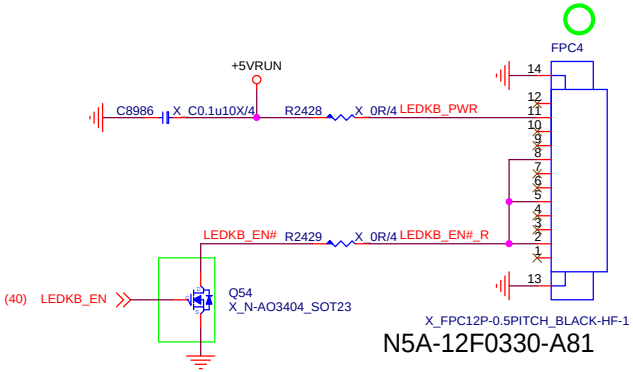
**3 Area of color KB_BOM Option :**

(1)MB_ID : Pull Low
(2)add BATCLK_M and BATDATA_M
(3)pin8 : +3VSUS
(4)pin9 : HP_R_ADC
(5)pin10 : HP_L_ADC
(6)pin12 : DIMM_ON




N5A-16F0210-A81

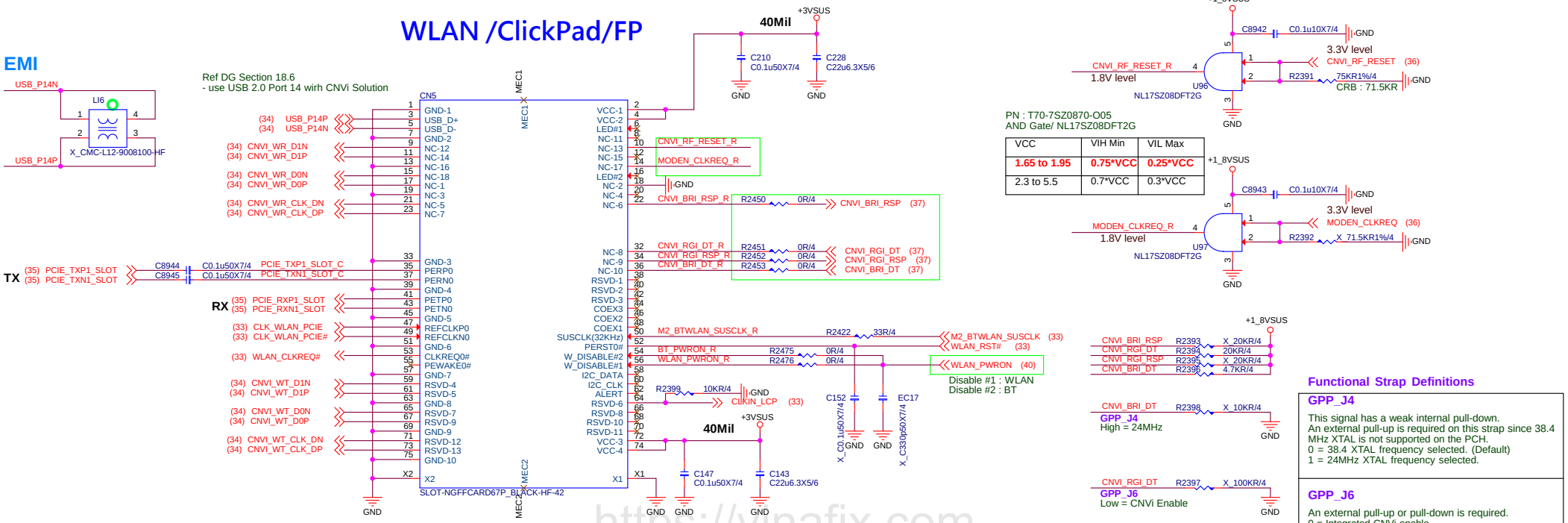
# White Color Keyboard Control




N5A-12F0330-A81

| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | |
| Title: USB2.0/Keyboard Control | | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B |
| Date: Tuesday, October 17, 2017 | Sheet 53 of 80 | |

# WLAN /ClickPad/FP




| VCC | VIH Min | VIL Max |
|---|---|---|
| 1.65 to 1.95 | 0.75*VCC | 0.25*VCC |
| 2.3 to 5.5 | 0.7*VCC | 0.3*VCC |

## Functional Strap Definitions

**GPP_J4**

This signal has a weak internal pull-down.
An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH.
0 = 38.4 XTAL frequency selected. (Default)
1 = 24MHz XTAL frequency selected.

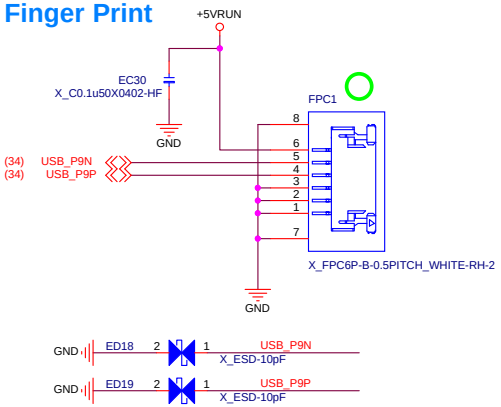
**GPP_J6**

An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

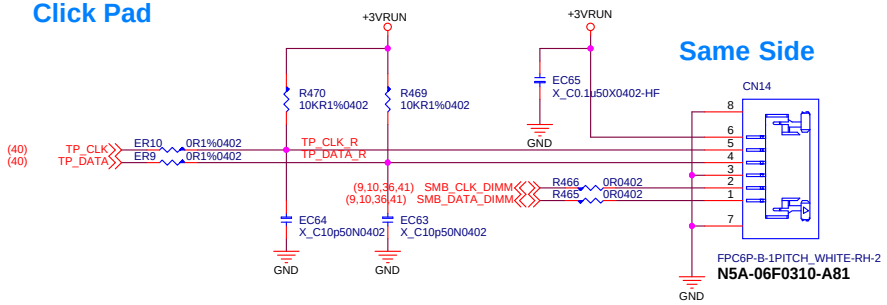
N15-0670520-L41
SLOT_NGFFCARD67_H2_15

https://vinafix.com

## Finger Print




## Click Pad



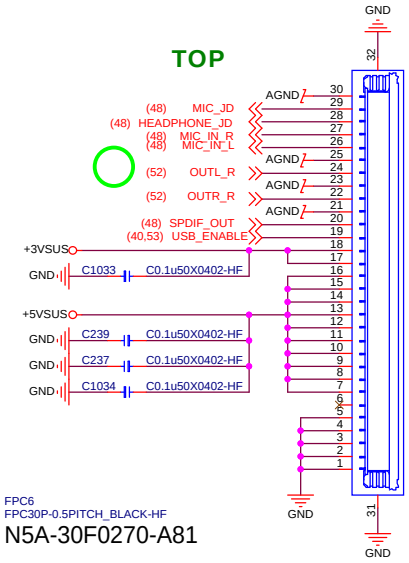

| | |
|---|---|
| Title | WLAN /ClickPad/FP |
| Size | Custom |
| Document Number | MS-16K51 |
| Rev | 0B |
| Date: | Tuesday, October 17, 2017 |
| Sheet | 54 of 80 |

MICRO-STAR INT'L CO.,LTD.

# 16K5 BTB CONN

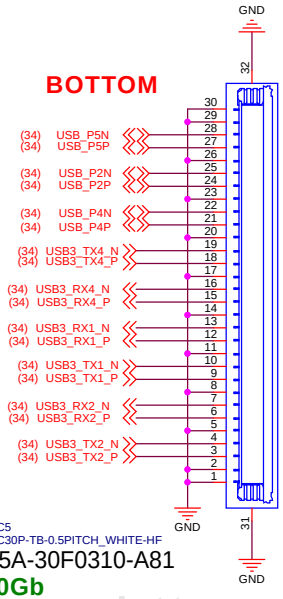
## (Audio CONN/USB3.0)

### TOP



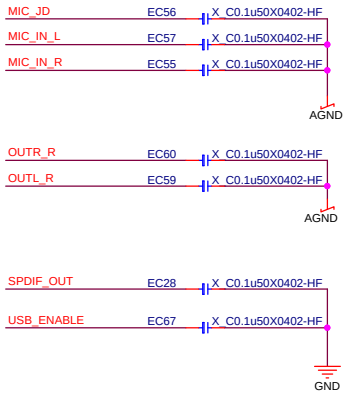

FPC6
FPC30P-0.5PITCH_BLACK-HF
N5A-30F0270-A81

### BOTTOM



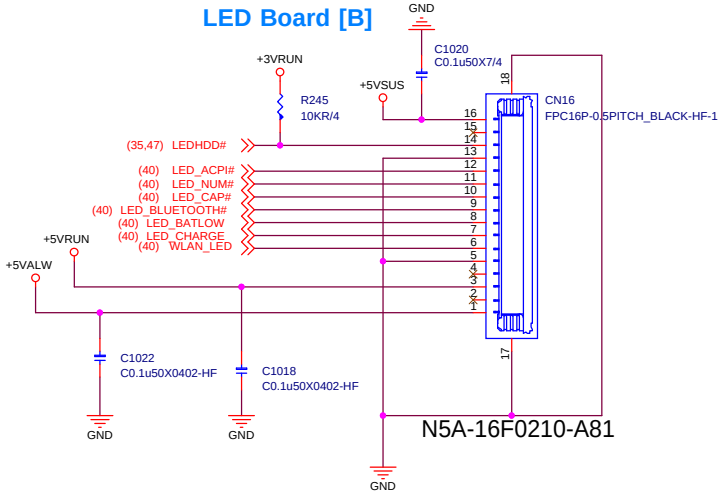

FPC5
FPC30P-TB-0.5PITCH_WHITE-HF
N5A-30F0310-A81
**10Gb**

### EMI



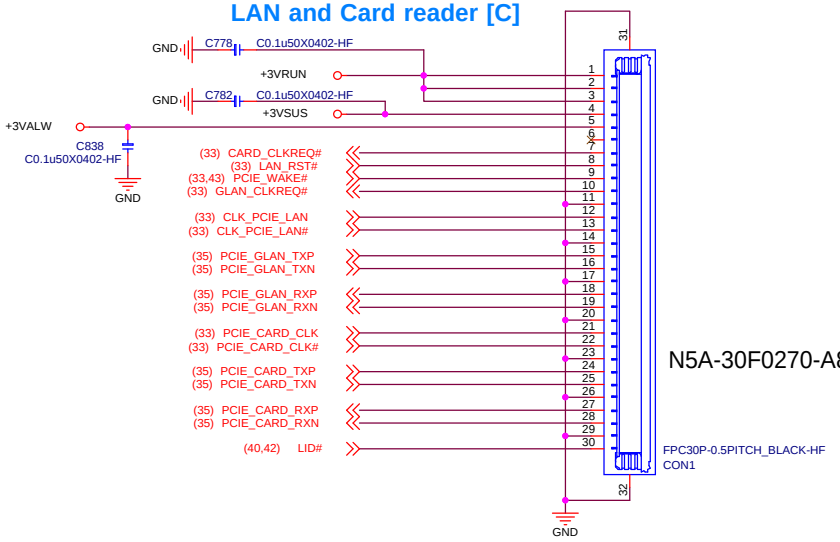

https://vinafix.com

### LED Board [B]




N5A-16F0210-A81

### LAN and Card reader [C]




N5A-30F0270-A81

FPC30P-0.5PITCH_BLACK-HF
CON1

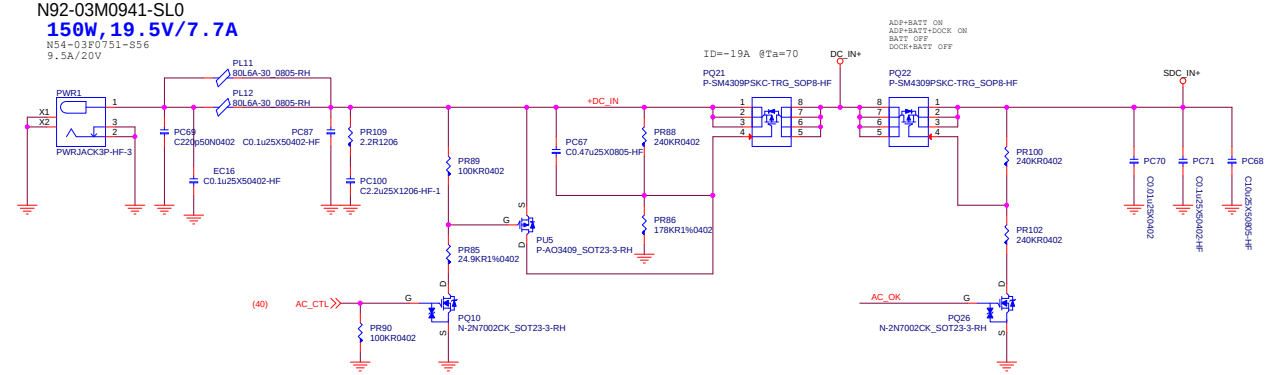
| | | |
|---|---|---|
| msi | MICRO-STAR INT'L CO.,LTD. | |
| Title | CPU FAN/BTB CONN | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B |
| Date: Thursday, October 05, 2017 | Sheet 55 of 80 | |

N92-03M0941-SL0

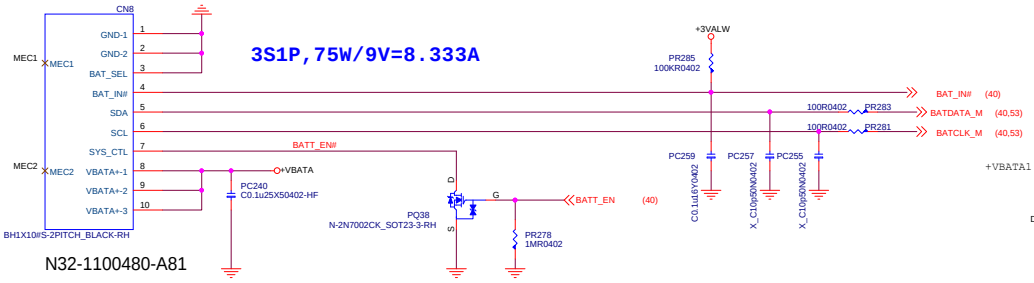
**150W,19.5V/7.7A**

N54-03F0751-S56

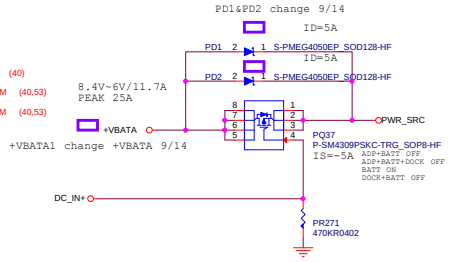
9.5A/20V

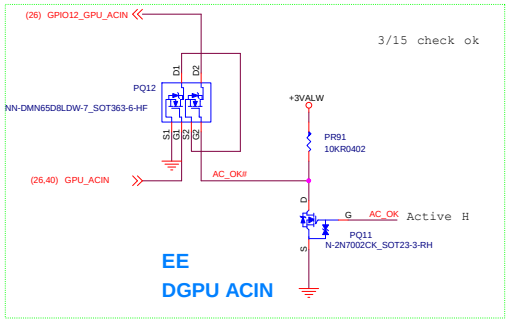



| AC_OK# | GPU_ACIN (EC control) | GPIO12_GPU_ACIN |
|---|---|---|
| 0 | 0 | AC |
| 0 | 1 | AC |
| 1 | 0 | AC |
| 1 | 1 | DC |

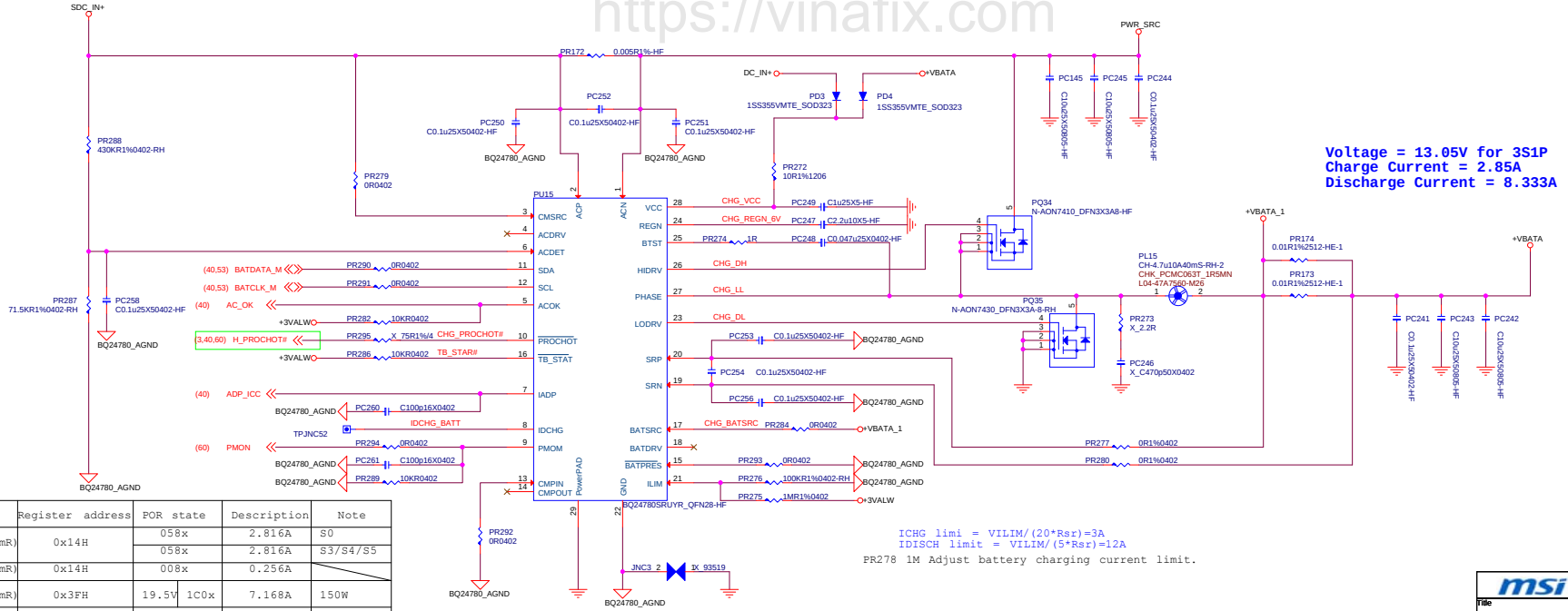



N32-1100480-A81




https://vinafix.com




**Voltage = 13.05V for 3S1P**
**Charge Current = 2.85A**
**Discharge Current = 8.333A**

| Register name | Register address | POR state | Description | Note |
|---|---|---|---|---|
| Charge current(5mR) | 0x14H | 058x | 2.816A | S0 |
| | | 058x | 2.816A | S3/S4/S5 |
| Prepare charge(5mR) | 0x14H | 008x | 0.256A | |
| Input current(10mR) | 0x3FH | 19.5V 1C0x | 7.168A | 150W |
| Charge voltage | 0x15H | 330x | 13.056V | 3S1P |
| Discharge current(5mR) | 0x39H | 06xx | 3.072A | BOOST current |

ICHG limi = VILIM/(20*Rsr)=3A
IDISCH limit = VILIM/(5*Rsr)=12A
PR278 1M Adjust battery charging current limit.

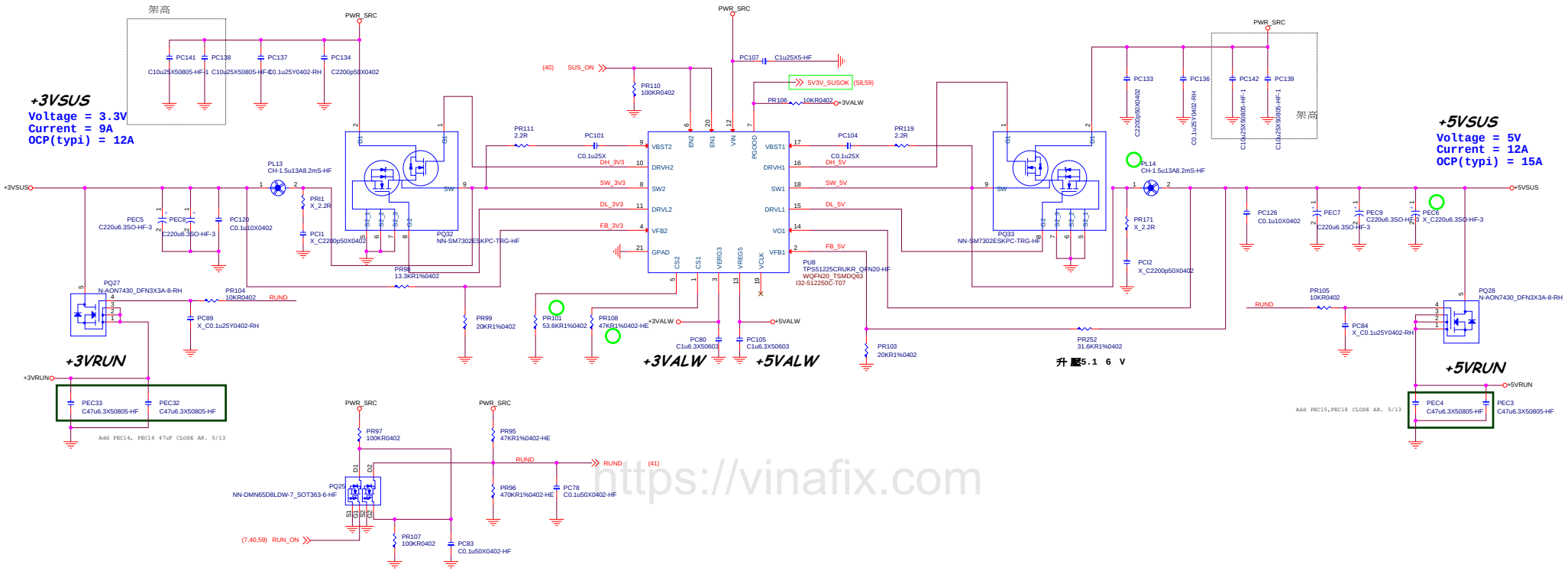
MICRO-STAR INT'L CO.,LTD.

Title: Battery select/Charger

Size: Custom | Document Number: MS-16K51 | Rev: 0B

Date: Friday, October 13, 2017 | Sheet 56 of 80

# System Power

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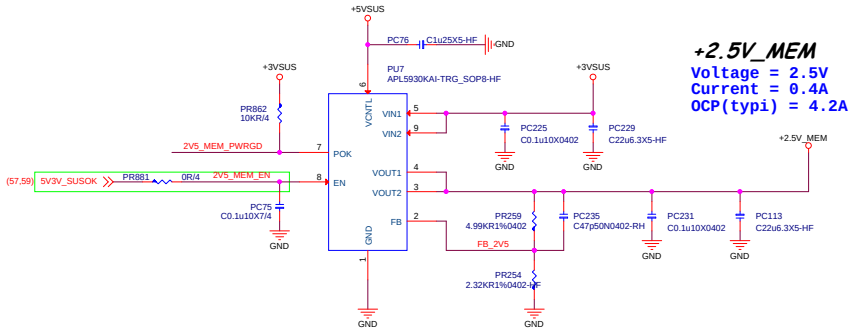
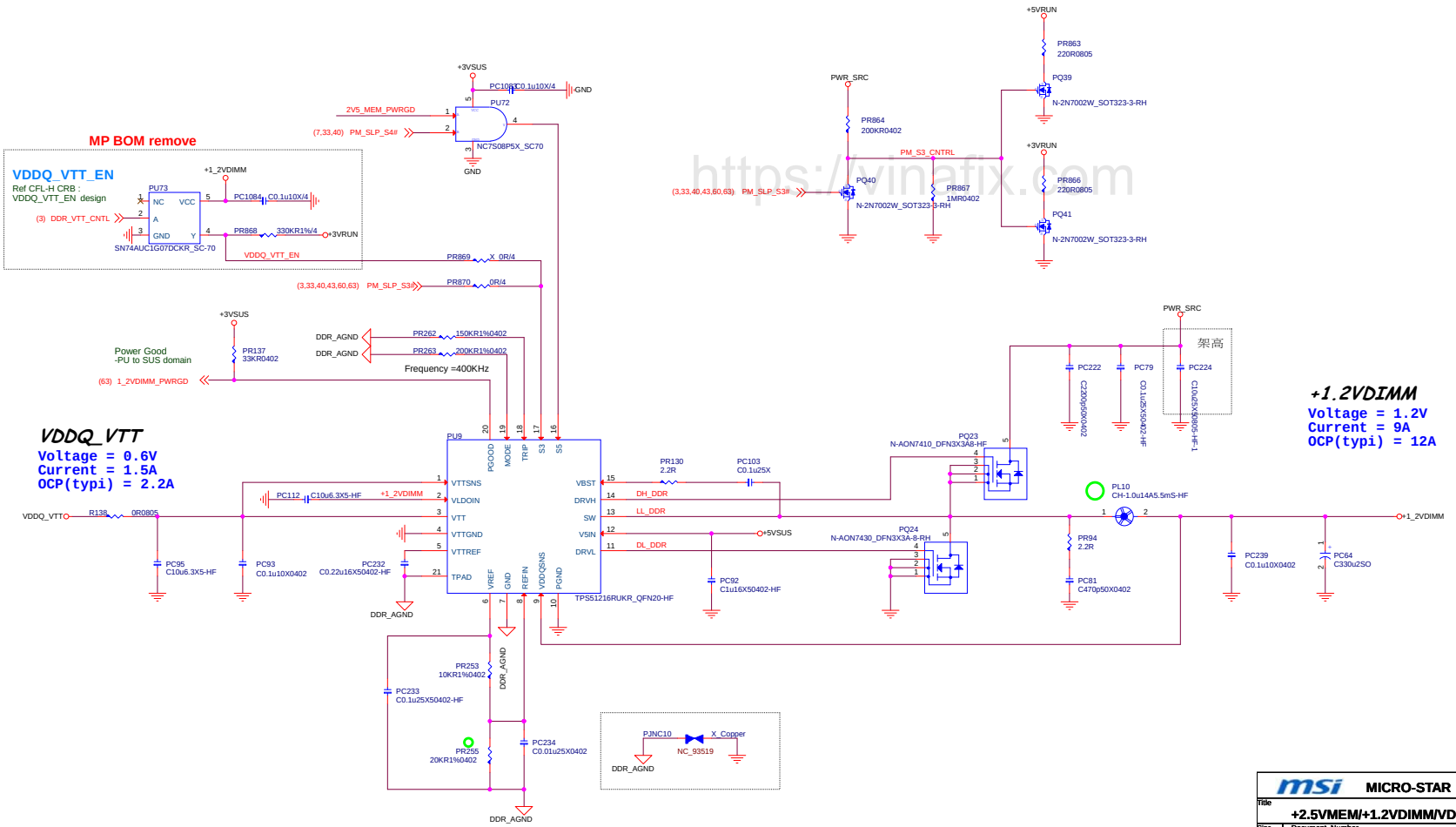
| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | |
| Title: System Power | | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B |
| Date: Friday, October 13, 2017 | Sheet 57 of 80 | |

# +2.5V_MEM (DDR4/Vpp)




***+2.5V_MEM***
**Voltage = 2.5V**
**Current = 0.4A**
**OCP(typi) = 4.2A**

# +1.2VDIMM / VDDQ_VTT(0.6V)




***+1.2VDIMM***
**Voltage = 1.2V**
**Current = 9A**
**OCP(typi) = 12A**

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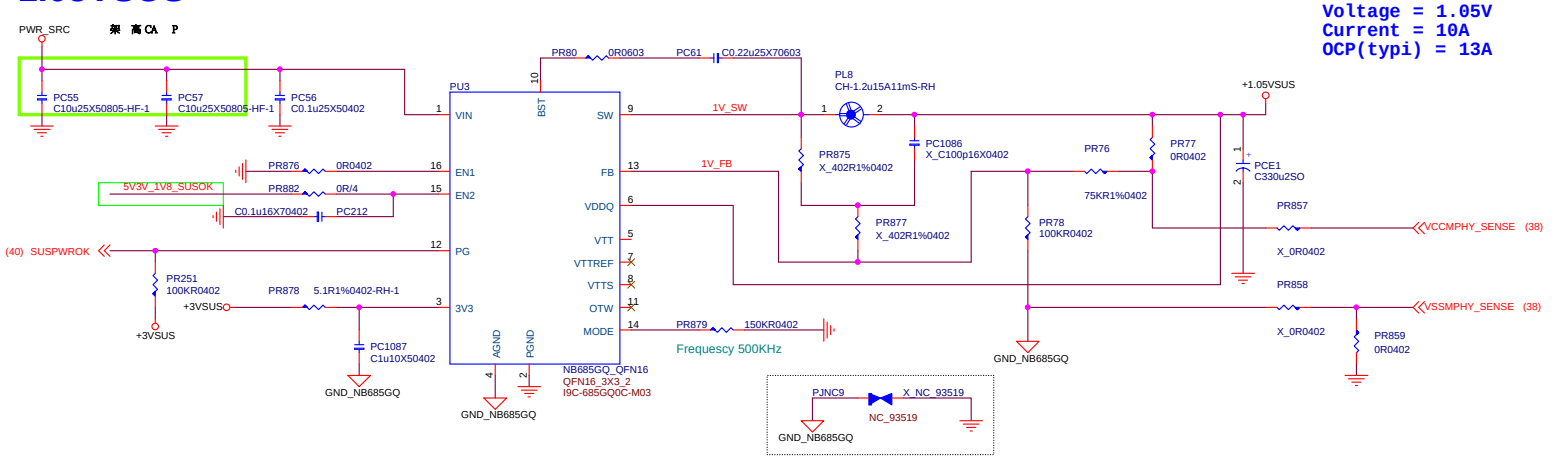
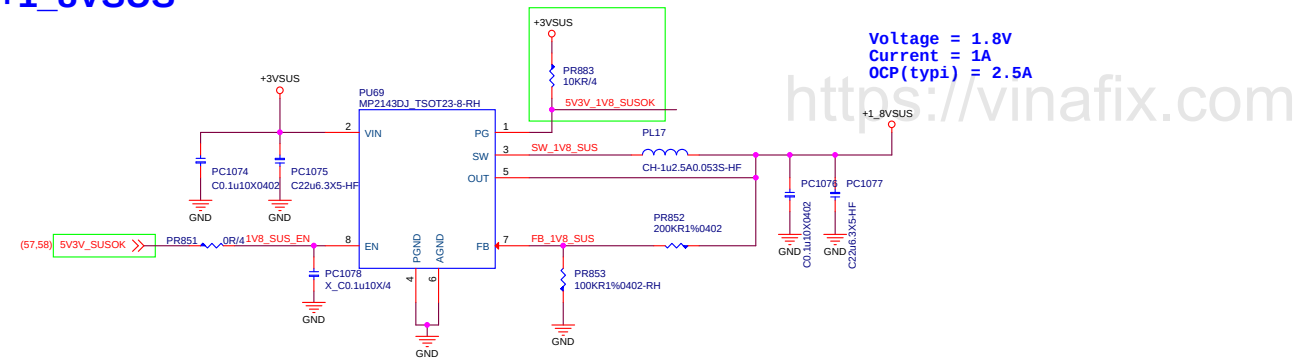
| | | |
|---|---|---|
| msi | MICRO-STAR INT'L CO.,LTD. | |
| Title | +2.5VMEM/+1.2VDIMM/VDDQ_VTT | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B |
| Date: Friday, October 13, 2017 | Sheet 58 of 80 | |

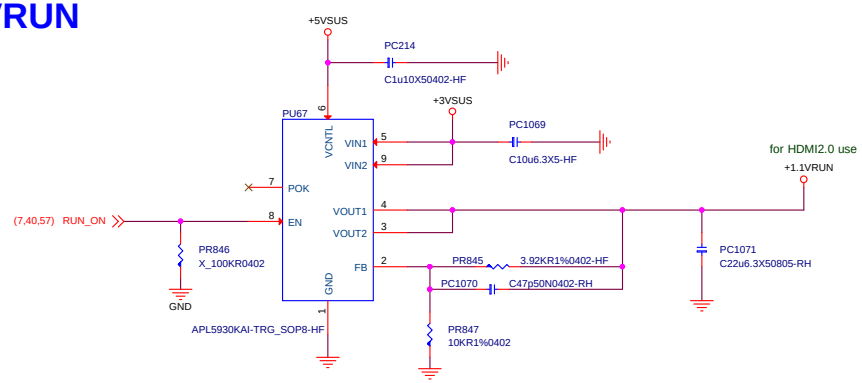
# +1.05VSUS




# +1_8VSUS



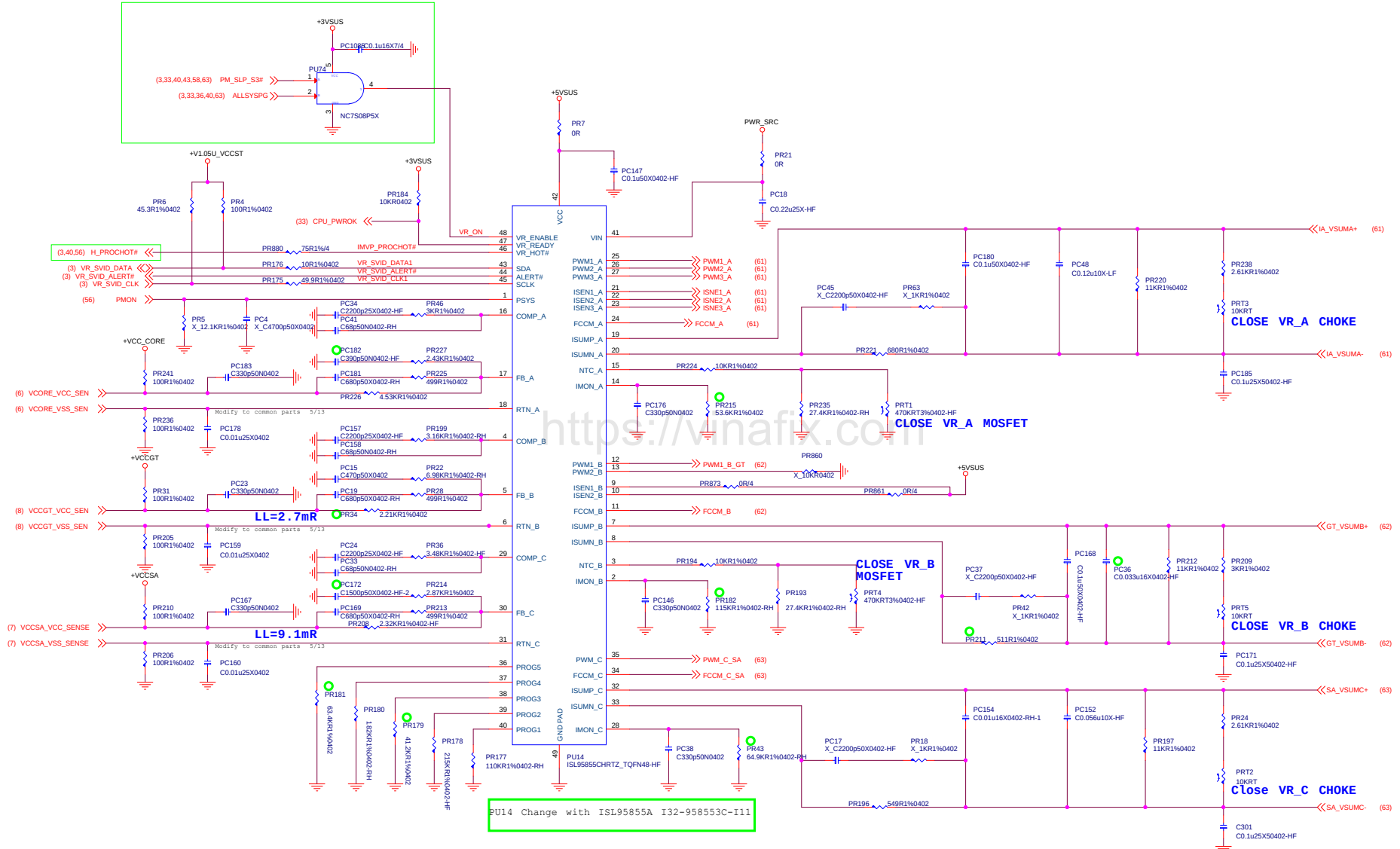

# +1.1VRUN




https://vinafix.com

| | | |
|---|---|---|
| msi | MICRO-STAR INT'L CO.,LTD. | |
| Title | +1.05VSUS/+1_8VSUS/+1.1VRUN | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B |
| Date: Thursday, October 05, 2017 | Sheet 59 of 80 | |

# Coffee Lake H-line 6+2 45W ISL95855A

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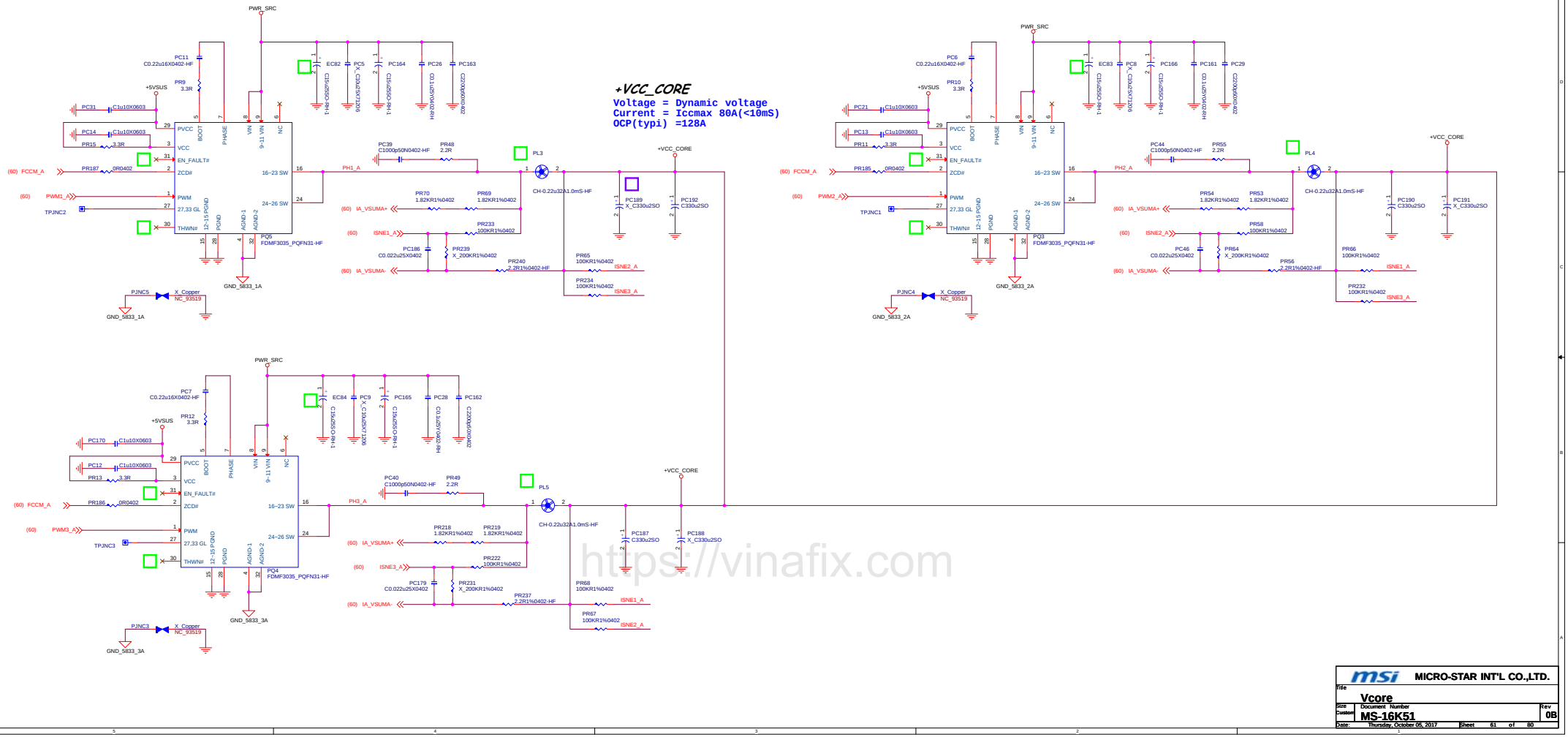
| | |
|---|---|
| MICRO-STAR INT'L CO.,LTD. | |
| Title | CFL-H 6+2 45W ISL95855A |
| Size: Custom | Document Number: MS-16K51 |
| Rev | 0B |
| Date: Thursday, October 05, 2017 | Sheet 60 of 80 |




| | |
|---|---|
| Title | Vcore |
| Size: Custom | Document Number: MS-16K51 |
| Rev | 0B |
| Date: | Thursday, October 05, 2017 |
| Sheet | 61 of 80 |

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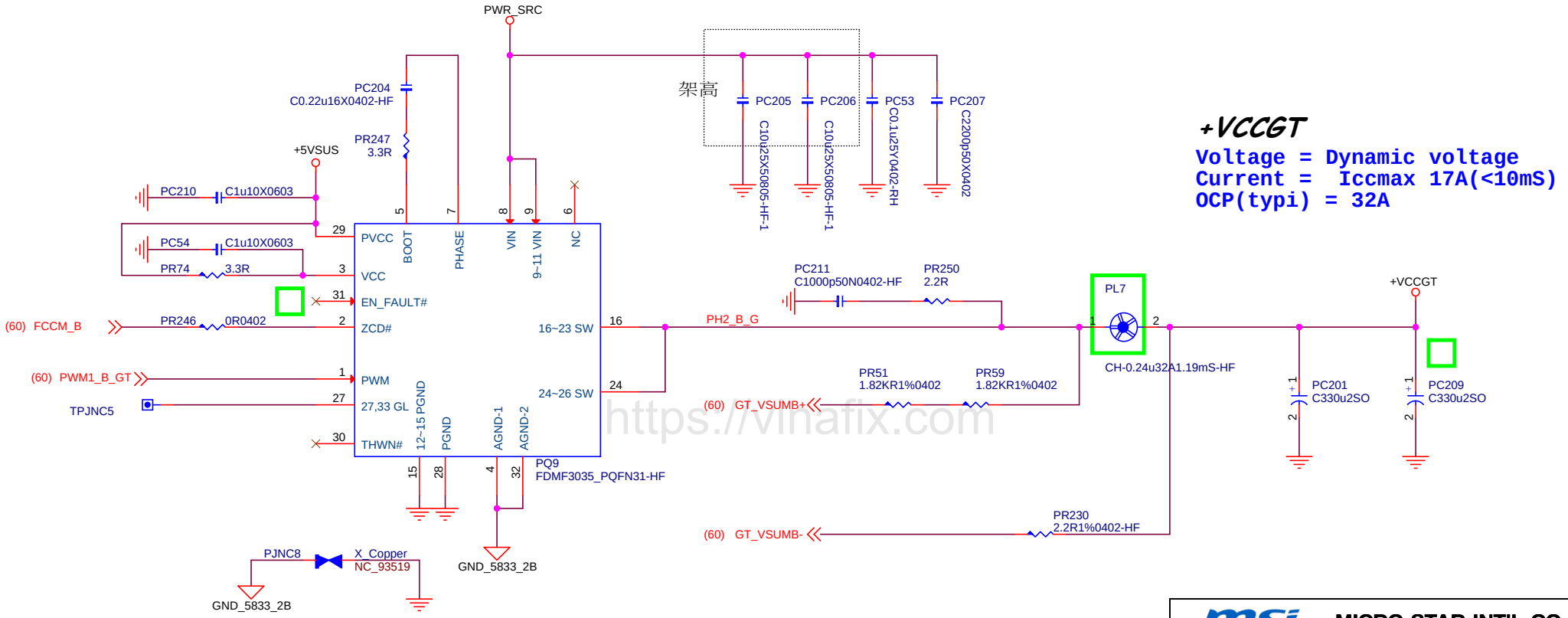
# +VCCGT

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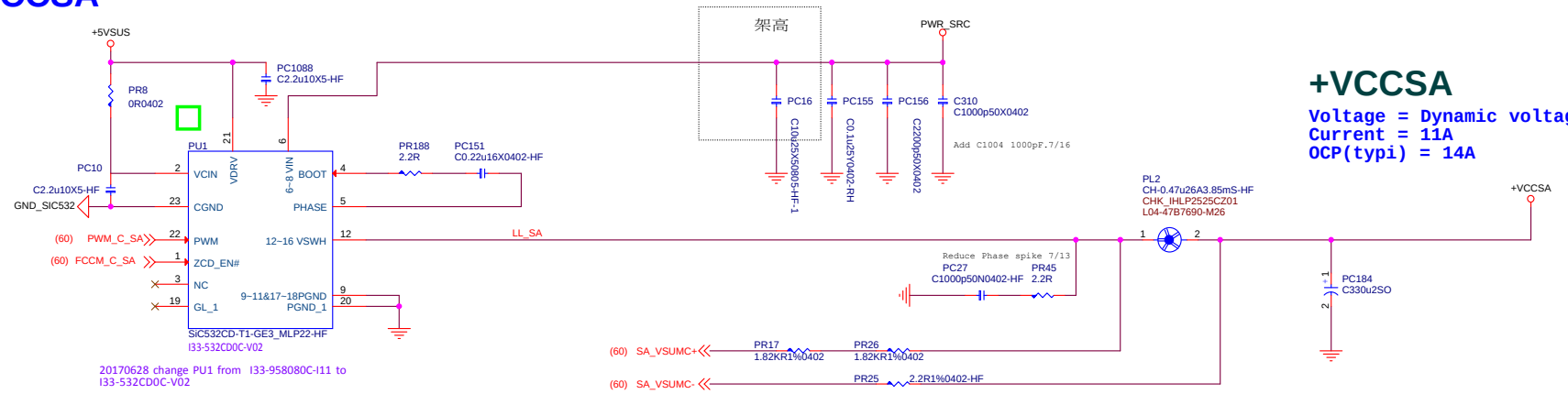
**+VCCGT**

**Voltage = Dynamic voltage**
**Current = Iccmax 17A(<10mS)**
**OCP(typi) = 32A**

MICRO-STAR INT'L CO.,LTD.

| | | |
|---|---|---|
| Title | VCCGT | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B |
| Date: Thursday, October 05, 2017 | Sheet 62 of 80 | |

# +VCCSA

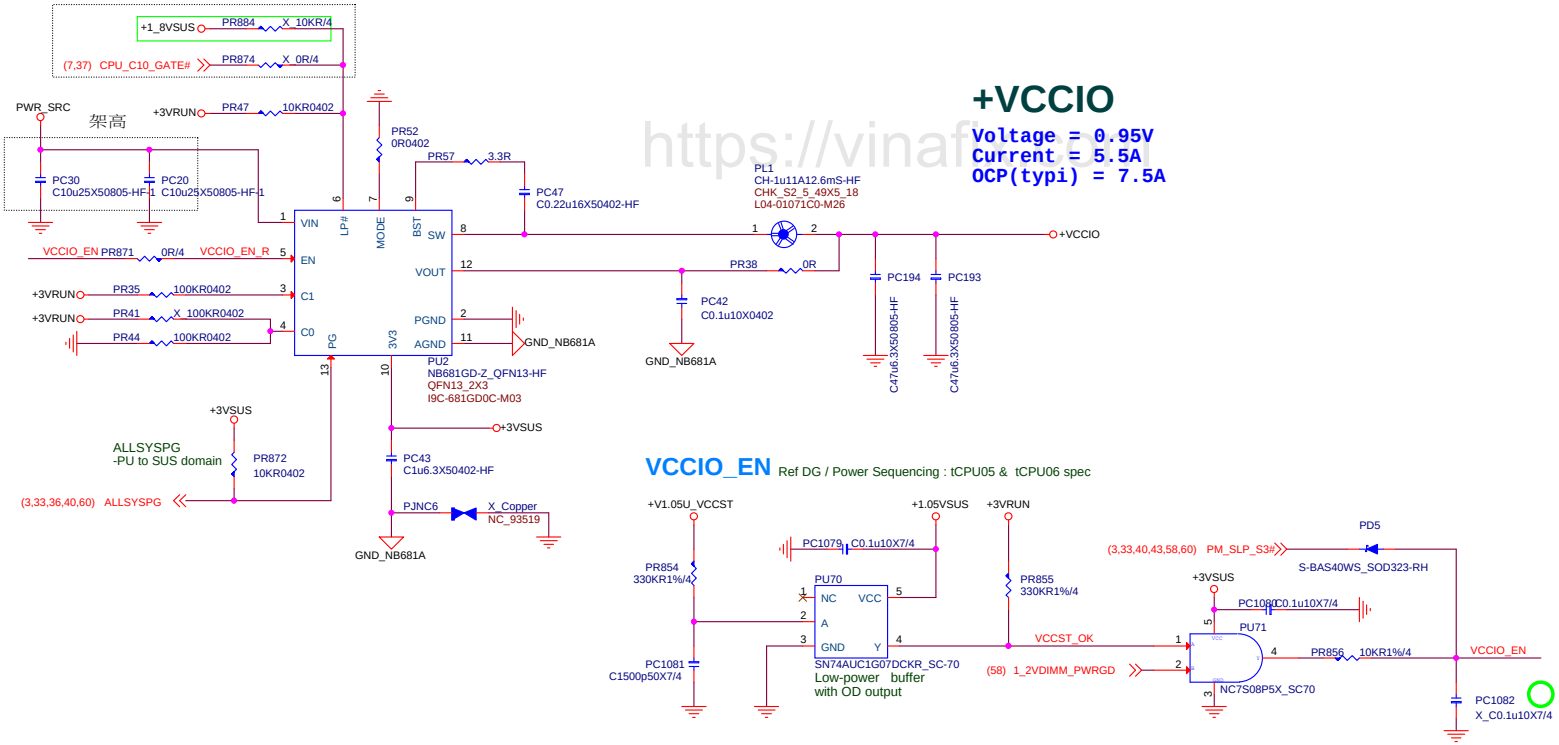



## +VCCSA

**Voltage = Dynamic voltage**
**Current = 11A**
**OCP(typi) = 14A**

# +VCCIO

Power Sequence spec tCPU27 :
CPU_C10_GATE# de-assertion to VCCSTG stable 10 < tCPU26 < 240 us




## +VCCIO

**Voltage = 0.95V**
**Current = 5.5A**
**OCP(typi) = 7.5A**

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## VCCIO_EN

Ref DG / Power Sequencing : tCPU05 & tCPU06 spec




| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | |
| Title: VCCSA/VCCIO | | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B |
| Date: Friday, October 13, 2017 | Sheet 63 of 80 | |

# DGPU POWER / UP9509P

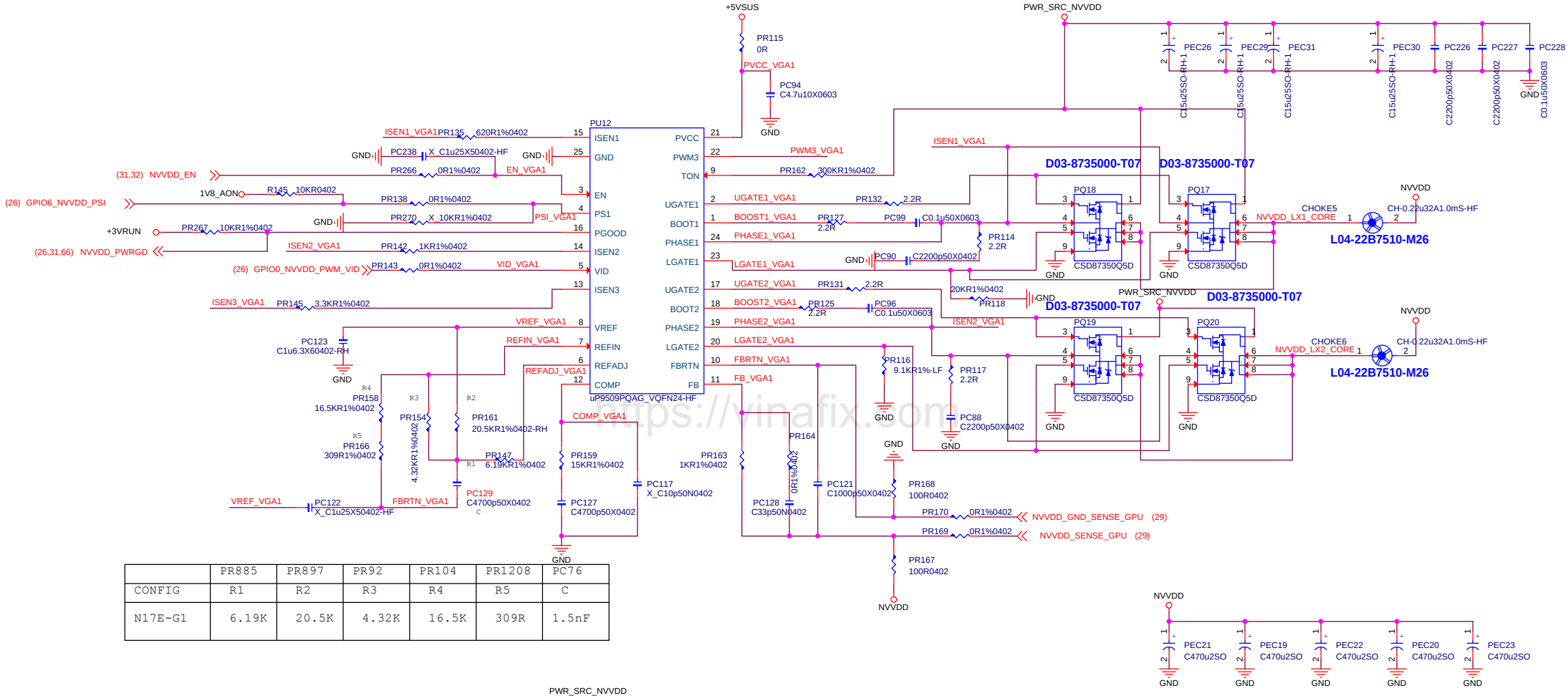
**EDP-Peak 136A**

**EDP-Con 58A**

# DGPU POWER NVVDD

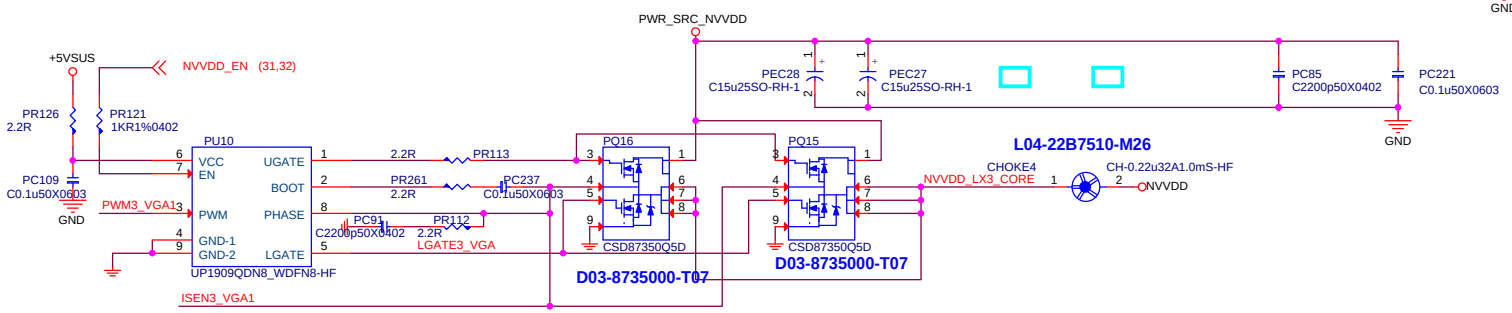
**VBoot:0.8V**

**Vmin:0.3V / Vmax:1.3V**




| | PR885 | PR897 | PR92 | PR104 | PR1208 | PC76 |
|---|---|---|---|---|---|---|
| CONFIG | R1 | R2 | R3 | R4 | R5 | C |
| N17E-G1 | 6.19K | 20.5K | 4.32K | 16.5K | 309R | 1.5nF |




| | |
|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD. |
| Title | NVVDD PWM IC (UP9509) |
| Size | Document Number: MS-16K51 |
| Rev | 0B |
| Date: | Sheet 64 of 80 |

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# DGPU POWER / UP1666P

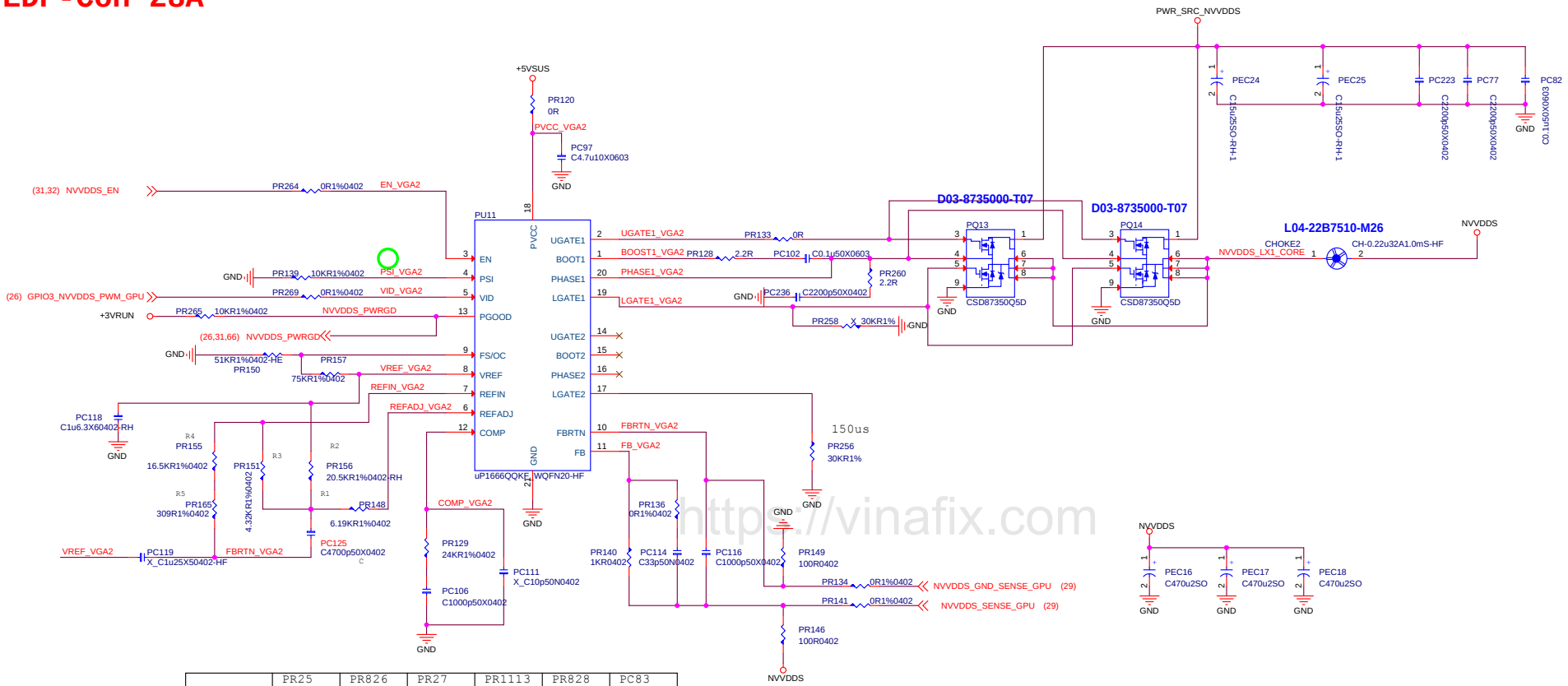
**EDP-Peak 74A**

**EDP-Con 28A**

# DGPU POWER NVVDDS

**VBoot:0.8V**

**Vmin:0.3V / Vmax:1.3V**




https://vinafix.com

| | PR25 | PR826 | PR27 | PR1113 | PR828 | PC83 |
|---|---|---|---|---|---|---|
| CONFIG | R1 | R2 | R3 | R4 | R5 | C |
| N17E-G1 | 6.19K | 20.5K | 4.32K | 16.5K | 309R | 1.5nF |

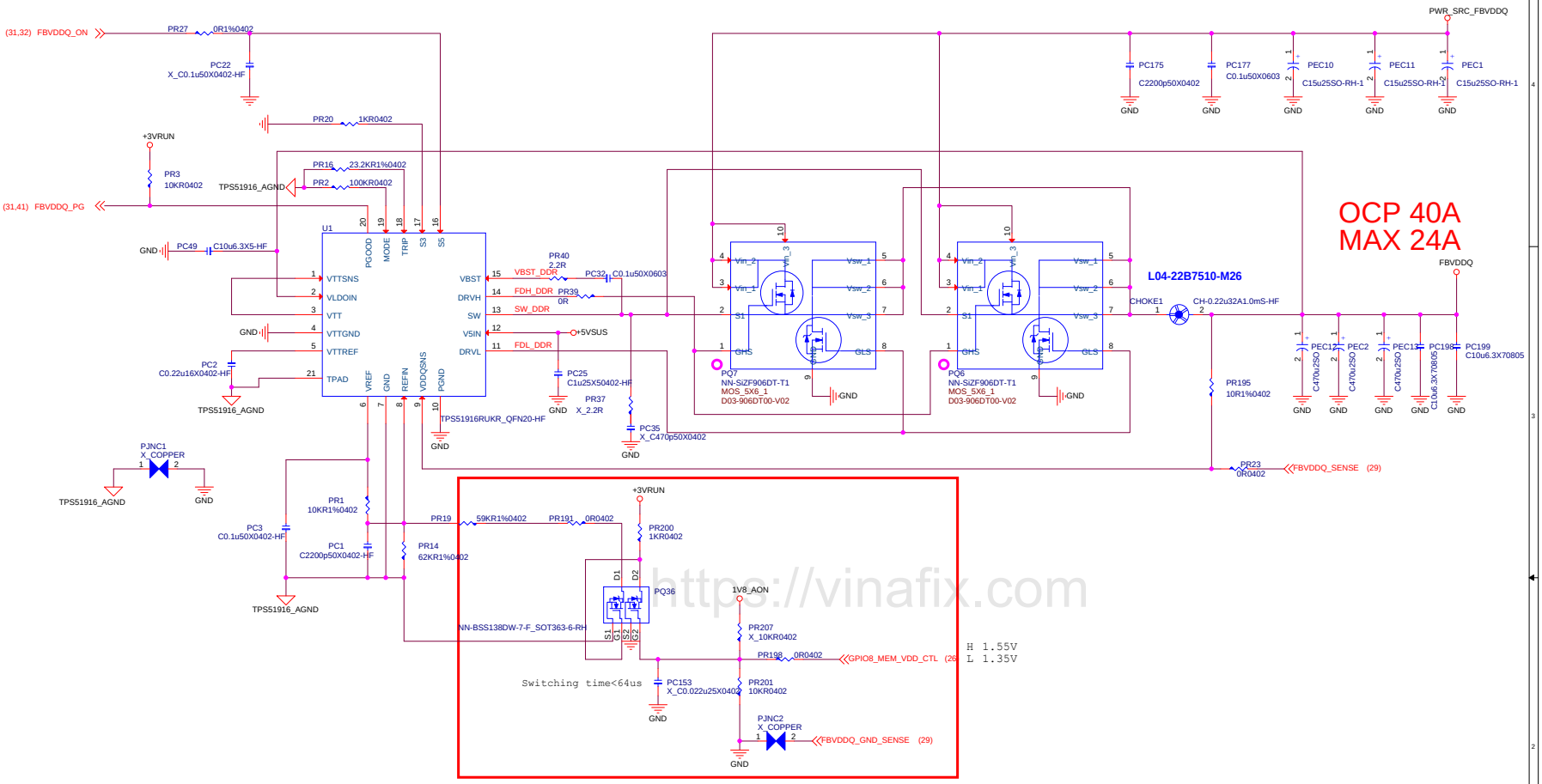
MSI MICRO-STAR INT'L CO.,LTD.

Title: NVVDDS

Size | Document Number: MS-16K51 | Rev: 0B

Date: | Sheet 65 of 80

# FBVDDQ

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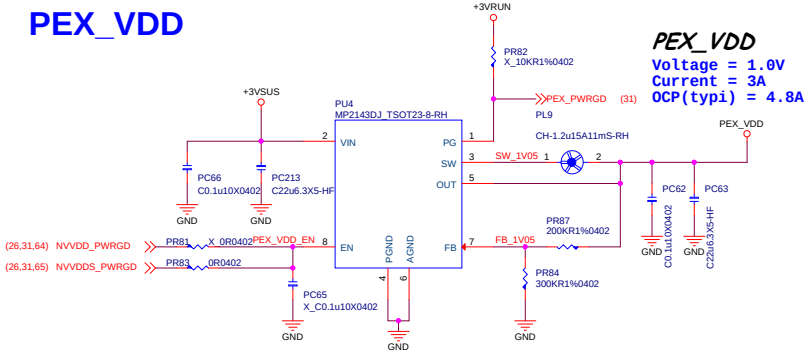
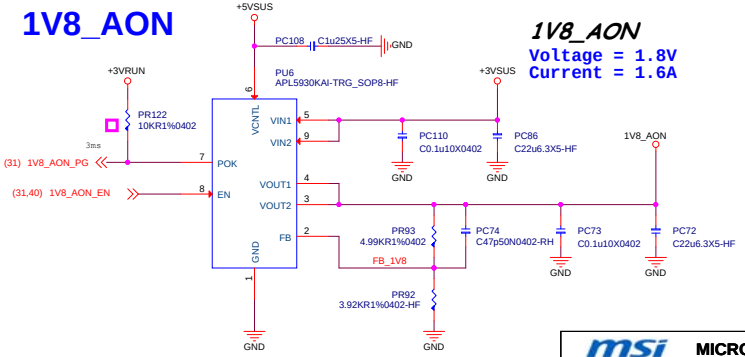
# PEX_VDD

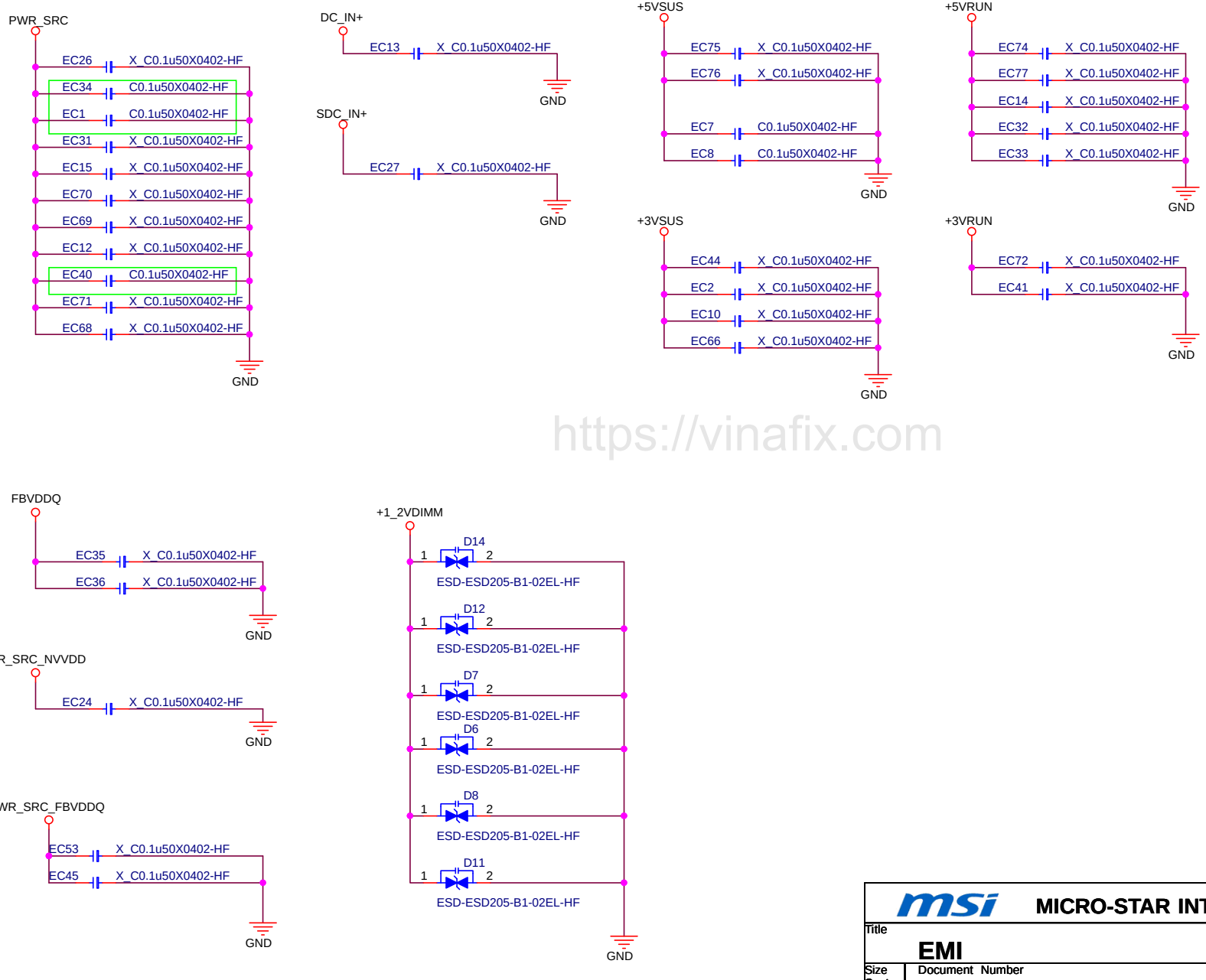



# 1V8_AON




| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | |
| Title: FBVDDQ/PEX_VDD/1V8_AON | | |
| Size | Document Number: MS-16K51 | Rev: 0B |
| Date: | Sheet 66 of 80 | |

# EMI




https://vinafix.com

| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | |
| Title: EMI | | |
| Size: Custom | Document Number: MS-16K51 | Rev: 0B |
| Date: Thursday, October 05, 2017 | Sheet 67 of 80 | |

## dGPU Holes

MGPU1 H_R185D169BR276_PB_N
MGPU2 H_R185D169BR276_PB_N
MGPU4 H_R185D169BR276_PB_N
MGPU3 H_R185D169BR276_PB_N

## CPU Holes

MCPU2 H_R276D169_PB_N
MCPU1 H_R276D169_PB_N
MCPU3 H_R276D169_PB_N

## CPU Bracket

UME5
CPU BKT
CPU BRACKET
307-6K50111-A89

## GPU Bracket

UME7
GPU BKT
GPU_BRACKET
307-7B10112-Y77

PCB1
PD0-16K510B-H73
PD0-16K510B-H73

FM22 FM5 FM17 FM32 FM15
FM11 FM27 FM4 FM12 FM34
FM29 FM23 FM25
FM16 FM8 FM37 FM28 FM20
FM1 FM26 FM9 FM21 FM36
FM7 FM3 FM10 FM6 FM35
FM39 FM30 FM31 FM2
FM18 FM13 FM38 FM14

MH6 X_H_R217D91_N
MH10 X_H_R197D118_PT_N
MH13 X_H_O236X256D91X110_N
MH14 X_H_R197D91_N
MH7 X_H_R217D91_N
MH9 X_H_R315D118_1_V3_N H_R315D118_V3_N
MH5 X_H_R217D91_N
MH11 H_R197D118_PT_N X_ME_ SCREW HOLE
MH17 X_H_NR118D118
MH18 X_H_NR118D118
MH20 X_H_NR118D118
MH19 X_H_NR118D118
MH4 X_H_R315D118_1_N
MH3 X_H_NR47D47_1_N
MH8 X_H_NR47D47_1_N
MH1 X_H_NR118D118_N
MH15 X_H_NR118D118_N
MH2 X_H_NR118D118_N
MH16 X_H_NR118D118_N

E4 X_HS-MS1011-RH
E1 X_HS-MS1011-RH
E3 X_HS-MS1011-RH

MH12
MXM Stand-off
E2B-16K1010-RH
SSD stand-off bottom

FM48 FM49 FM50 FM54
FM51 FM52 FM53 FM55

UME1
HDMI Lable
X_HDMI ROYALTY
Y01-RHDMI03-000

UME2
BIOS Lable
X_UEFI_CODE_BIOS_LABEL
G51-N1CO041-A09

For MP

UME24
Y01-REMPAS1-000
EMPASS_USB20

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## 17B51 BOM

| | | | | | |
|---|---|---|---|---|---|
| UME10 E2P-7B12211-Y42 X_ALFOIL MYLAR | UME12 E2P-7B12411-Y40 X_RUBBER | UME25 E2Y-7B12311-Y40 X_RUBBER | UME26 E2Y-7B12311-Y40 X_RUBBER | UME27 E2Y-7B12311-Y40 X_RUBBER | UME28 E2Y-7B12311-Y40 X_RUBBER |
| UME11 E2P-7B12611-G40 X_MYLAR | | UME33 E2Y-7B12311-Y40 X_RUBBER | UME34 E2Y-7B12311-Y40 X_RUBBER | UME35 E2Y-7B12311-Y40 X_RUBBER | UME36 E2Y-7B12311-Y40 X_RUBBER |

## 16K51 BOM

UME9
MB PC
MB_PC
E2P-6K11611-Y42

RU2
E2M-3570611-G40
MECH

| | | | |
|---|---|---|---|
| UME29 E2Y-6K21111-Y40 RUBBER | UME30 E2Y-6K21111-Y40 RUBBER | UME31 E2Y-6K21111-Y40 RUBBER | UME32 E2Y-6K21111-Y40 RUBBER |
| UME37 E2Y-6K21111-Y40 RUBBER | UME38 E2Y-6K21111-Y40 RUBBER | UME39 E2Y-6K21111-Y40 RUBBER | UME40 E2Y-6K21111-Y40 RUBBER |

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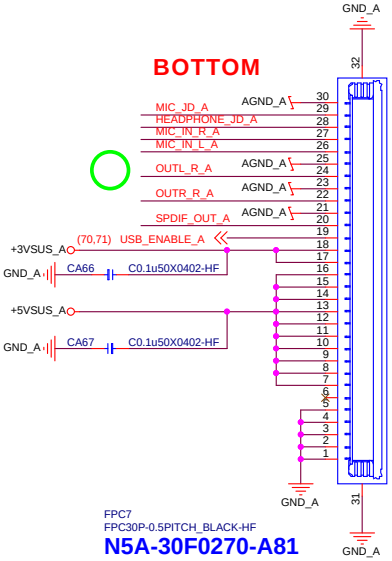
Title: Screw/ME
Size: Document Number: MS-16K51 Rev: 0B
Date: Thursday, October 05, 2017 Sheet 68 of 80

# 16K5-A Board (Audio CONN)

## BTB Connector From MB

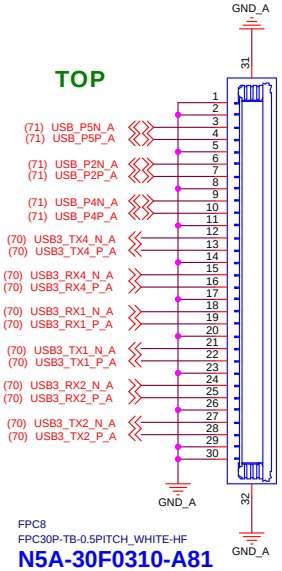
CONN Pin Current Capability : ???A/Pin

### BOTTOM




**N5A-30F0270-A81**

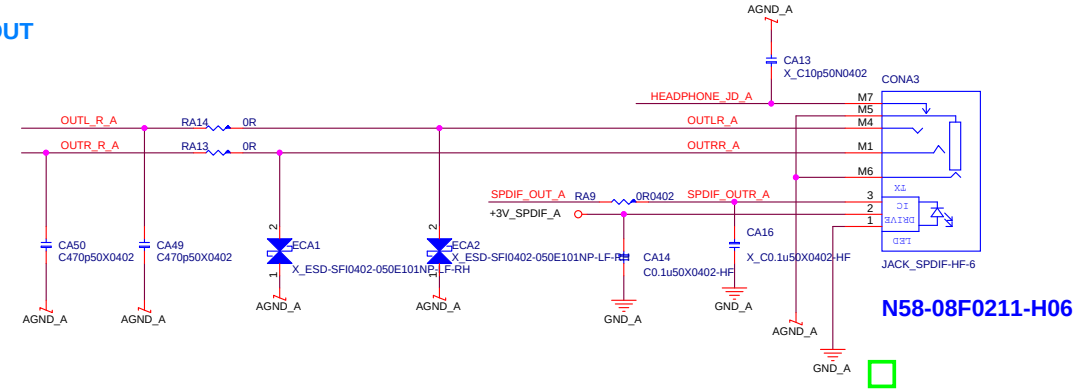
### TOP




**N5A-30F0310-A81**

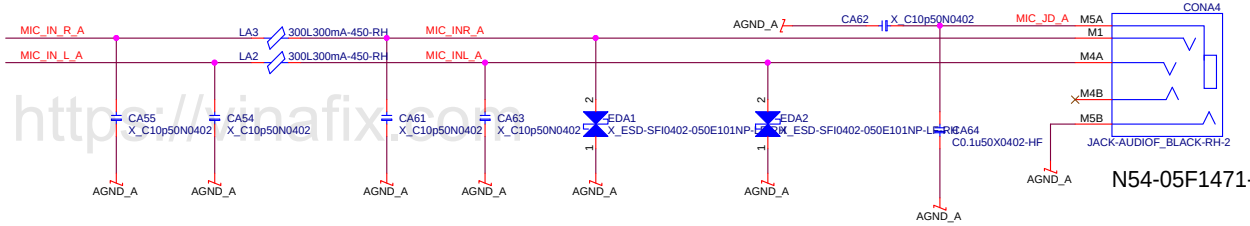
**10Gb**

## HP OUT / SPDIF OUT




**N58-08F0211-H06**

## MIC IN

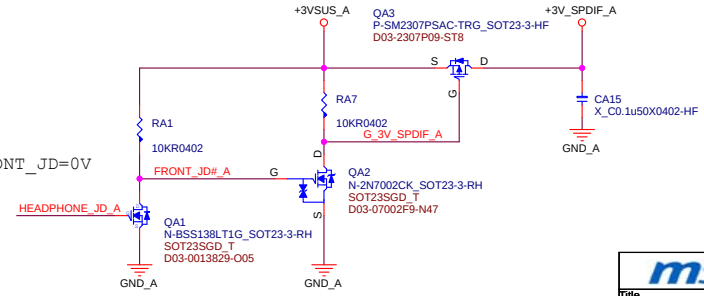



N54-05F1471-H06

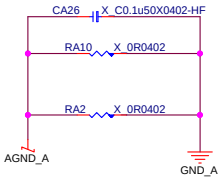
https://inafix.com

## SPDIF Power

VGS_ON : -1V~-2V

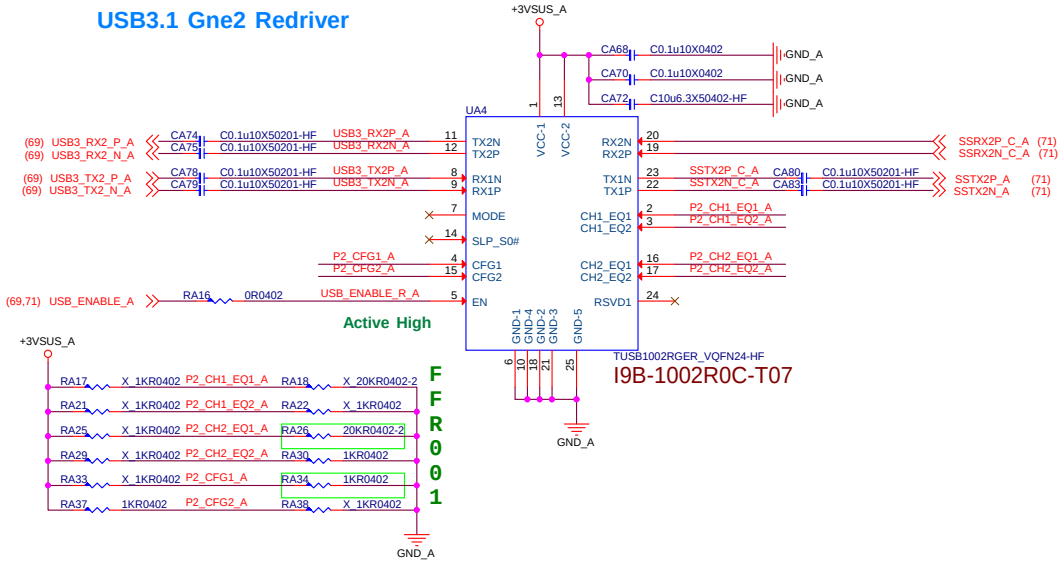


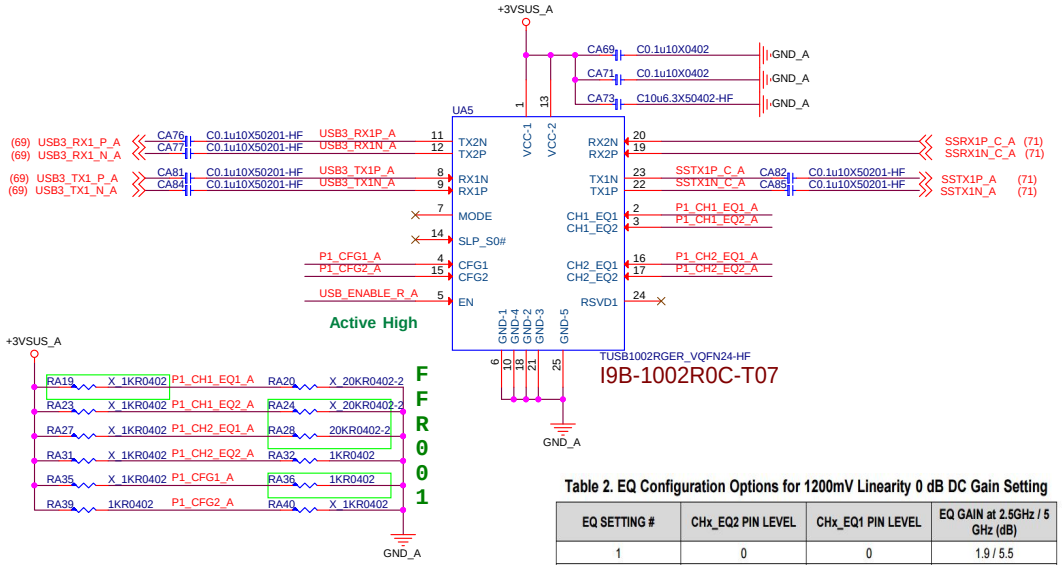

## EMI

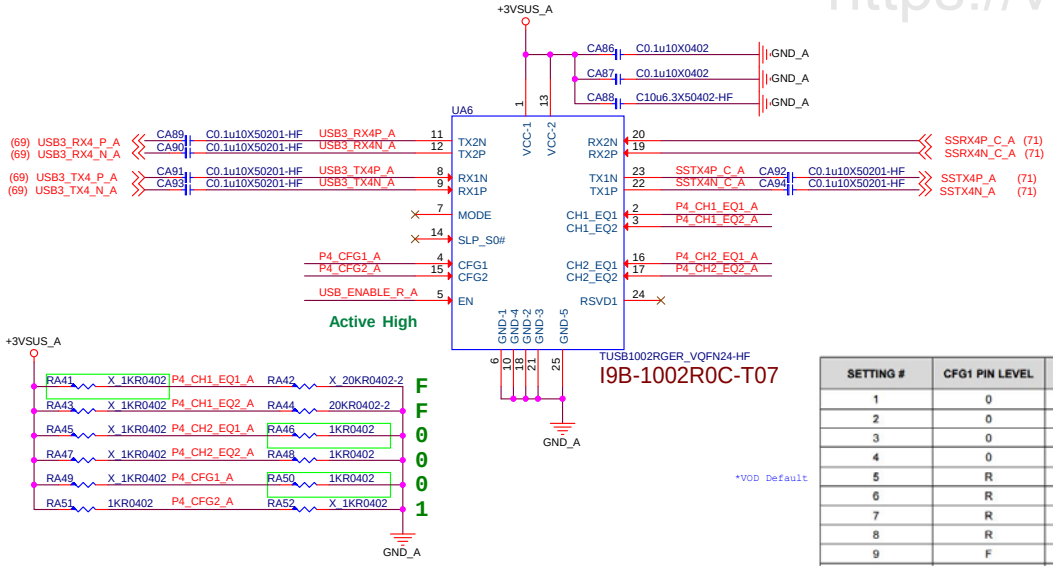


| | | | |
|---|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | | |
| Title: [A] Audio | | | |
| Size: Custom | Document Number: MS-16K5A | | Rev: 0B |
| Date: Thursday, October 05, 2017 | | Sheet 69 of 80 | |

## USB3.1 Gne2 Redriver




https://vinafix.com

**Table 2. EQ Configuration Options for 1200mV Linearity 0 dB DC Gain Setting**

| EQ SETTING # | CHx_EQ2 PIN LEVEL | CHx_EQ1 PIN LEVEL | EQ GAIN at 2.5GHz / 5 GHz (dB) |
|---|---|---|---|
| 1 | 0 | 0 | 1.9 / 5.5 |
| 2 | 0 | R | 2.8 / 7.1 |
| 3 | 0 | F | 3.5 / 8.2 |
| 4 | 0 | 1 | 4.4 / 9.3 |
| 5 | R | 0 | 5.0 / 10.2 |
| 6 | R | R | 5.8 / 11.1 |
| 7 | R | F | 6.4 / 11.8 |
| 8 | R | 1 | 7.1 / 12.6 |
| 9 | F | 0 | 7.6 / 13.1 |
| 10 | F | R | 8.2 / 13.8 |
| 11 | F | F | 8.7 / 14.3 |
| 12 | F | 1 | 9.2 / 14.8 |
| 13 | 1 | 0 | 9.6 / 15.2 |
| 14 | 1 | R | 10.1 / 15.6 |
| 15 | 1 | F | Reserved. |
| 16 | 1 | 1 | Reserved. |

*CH1 Default

*CH2 Default

**Table 3. VOD Linear Range and DC Gain**

| SETTING # | CFG1 PIN LEVEL | CFG2 PIN LEVEL | CH1 DC GAIN (dB) | CH2 DC GAIN (dB) | CH1 $V_{OD}$ LINEAR RANGE (mVpp) | CH2 $V_{OD}$ LINEAR RANGE (mVpp) |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | +1 | 0 | 900 | 900 |
| 2 | 0 | R | 0 | +1 | 900 | 900 |
| 3 | 0 | F | 0 | 0 | 900 | 900 |
| 4 | 0 | 1 | +1 | +1 | 900 | 900 |
| 5 | R | 0 | 0 | 0 | 1000 | 1000 |
| 6 | R | R | +1 | 0 | 1000 | 1000 |
| 7 | R | F | 0 | -1 | 1000 | 1000 |
| 8 | R | 1 | +2 | +2 | 1000 | 1000 |
| 9 | F | 0 | -1 | -1 | 1200 | 1200 |
| 10 | F | R | -2 | -2 | 1200 | 1200 |
| 11 | F | F | 0 | 0 | 1200 | 1200 |
| 12 | F | 1 | +1 | +1 | 1200 | 1200 |
| 13 | 1 | 0 | -1 | 0 | 1200 | 1200 |
| 14 | 1 | R | 0 | -1 | 1200 | 1200 |
| 15 | 1 | F | 0 | +1 | 1200 | 1200 |
| 16 | 1 | 1 | +1 | 0 | 1200 | 1200 |

*VOD Default

**Table 1. 4-Level Control Pin Settings**

| LEVEL | SETTINGS |
|---|---|
| 0 | Option 1: Tie 1 KΩ 5% to GND.<br>Option 2: Tie directly to GND. |
| R | Tie 20 KΩ 5% to GND. |
| F | Float (leave pin open) |
| 1 | Option 1: Tie 1 KΩ 5% to $V_{CC}$.<br>Option 2: Tie directly to $V_{CC}$. |

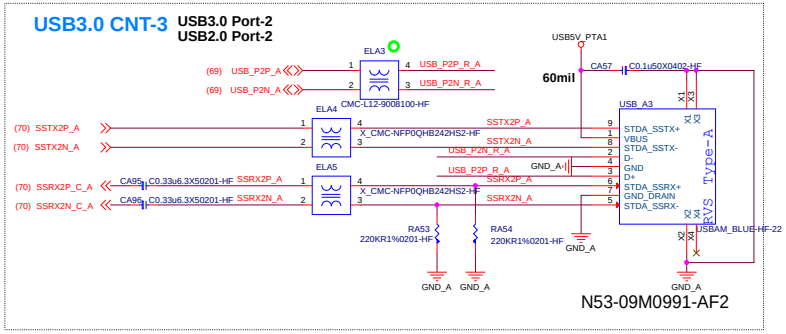
MICRO-STAR INT'L CO.,LTD.

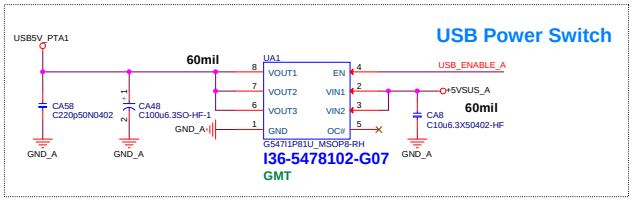
Title: [A] USB3.1 GEN2 REDRIVER

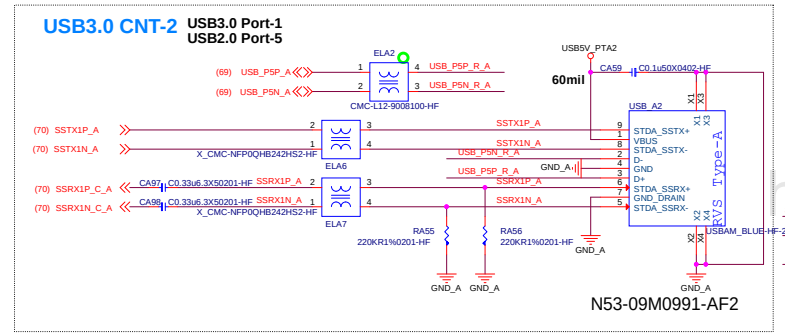
Size: Custom | Document Number: MS-16K5A | Rev: 0B

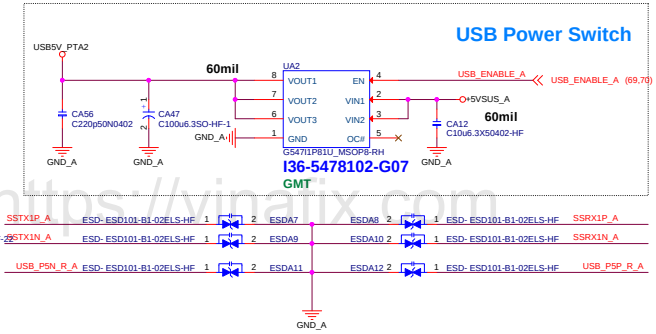
Date: Tuesday, October 17, 2017 | Sheet 70 of 80

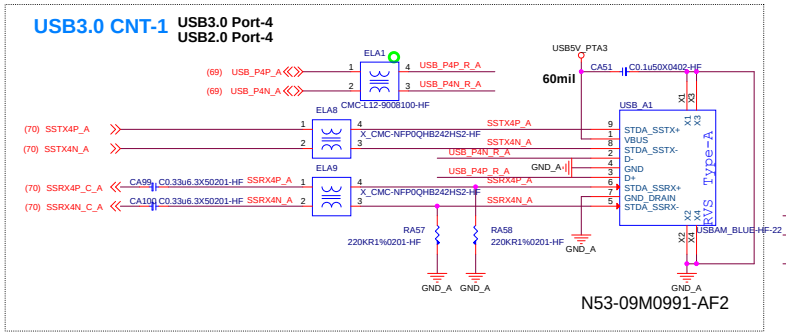
# [A] USB3.0 CNT-2/-3

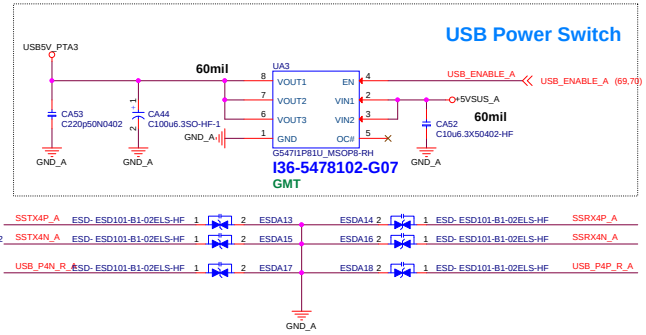



MYLARA4
16K5A BOM
E2P-6K50211-G40
USB_MYLAR

PCBA1
PD0-16K5A0B-H73
PD0-16K5A0B-H73

H_NR47D47_1
MA3
X_H_NR47D47_1
H_NR47D47_1
MA1
X_H_NR47D47_1

H_O197X236D91X130_N
MA2
X_H_O197X236D91X130_N
MA4
X_H_R276D118_PT_V3_N
H_R276D118_PT_V3_N
GND2_A
CA65
C0.1u50X0402-HF
RA15
X_10KR0402
AGND_A

FMA1
FMA4

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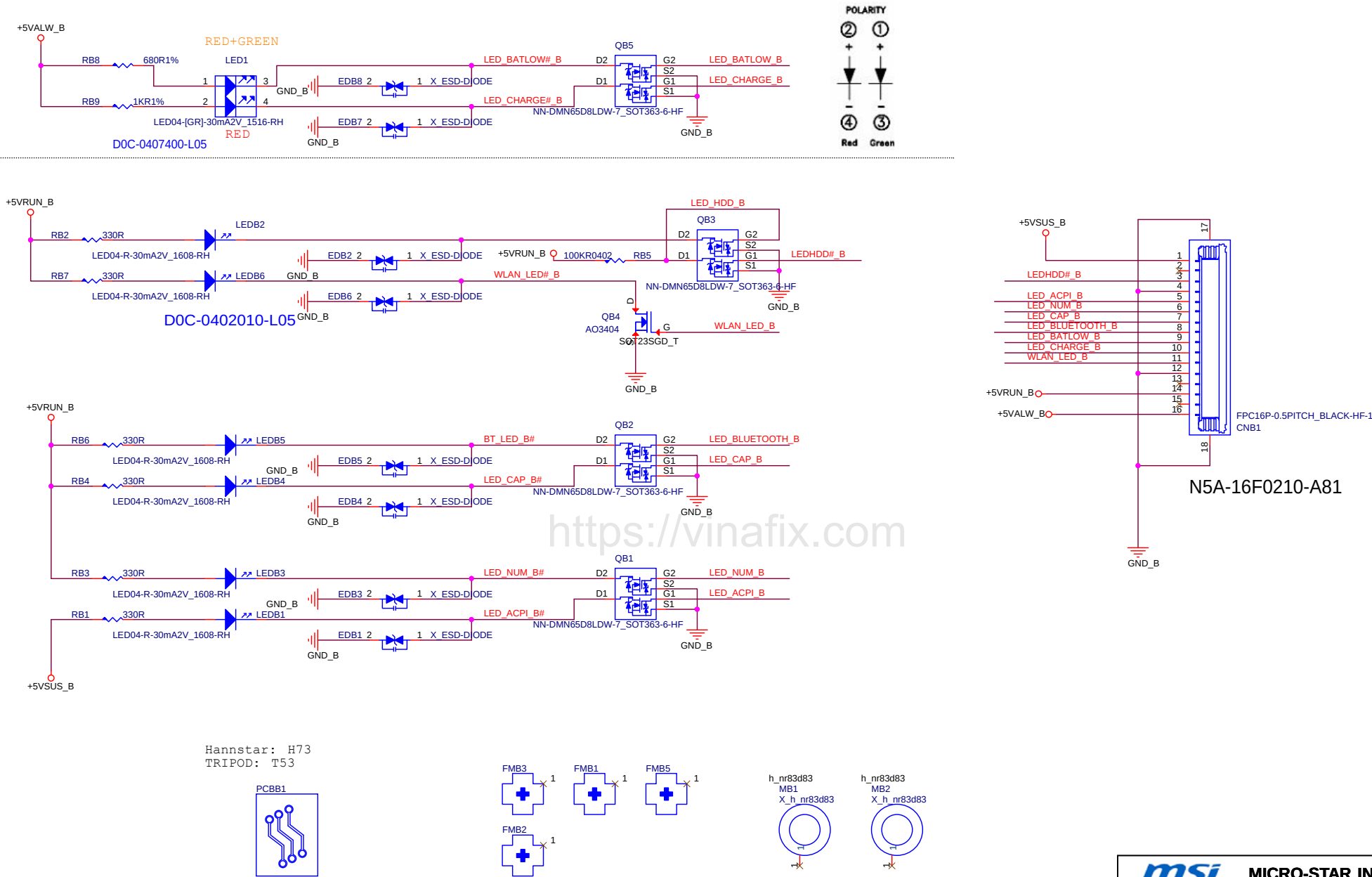
MICRO-STAR INT'L CO.,LTD.

Title: [A] USB3.0 CNT-3/-4

Size: Custom | Document Number: MS-16K5A | Rev: 0B

Date: Thursday, October 05, 2017 | Sheet 71 of 80

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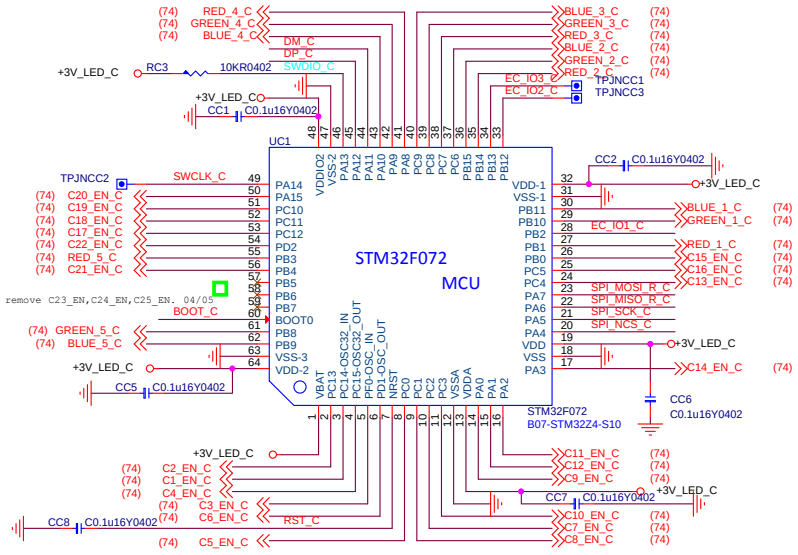
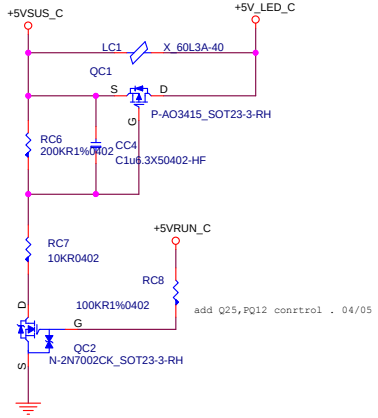
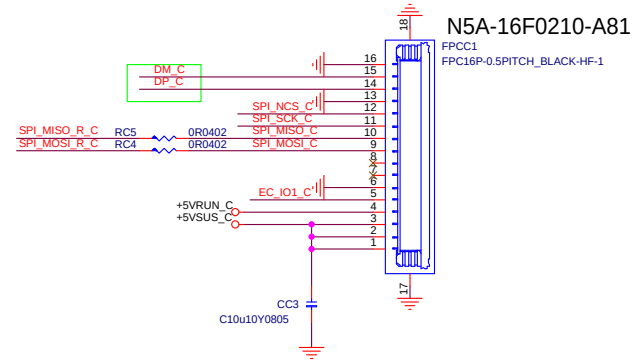
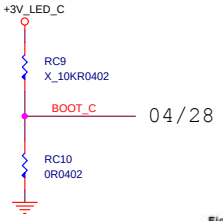
| | | | |
|---|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | | |
| Title: [B] LED | | | |
| Size: B | Document Number: MS-16K5B | | Rev: 0B |
| Date: Tuesday, October 03, 2017 | Sheet 72 of 80 | | |



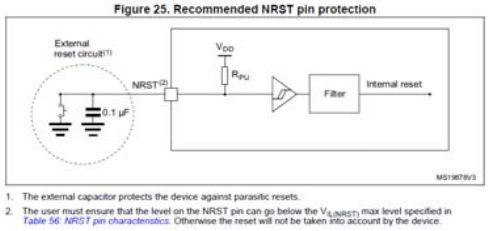



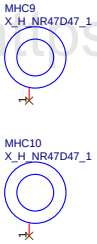

*Confirm Pin 1 position*

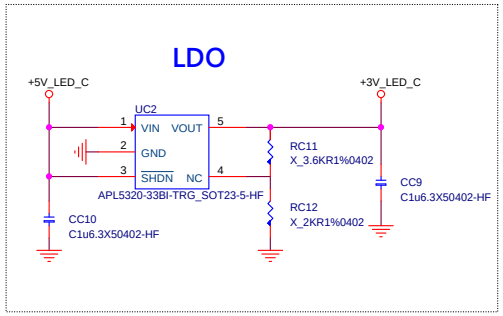


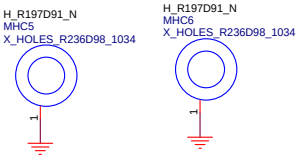

04/28 add Boot net and resistor




1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 56: NRST pin characteristics. Otherwise the reset will not be taken into account by the device.

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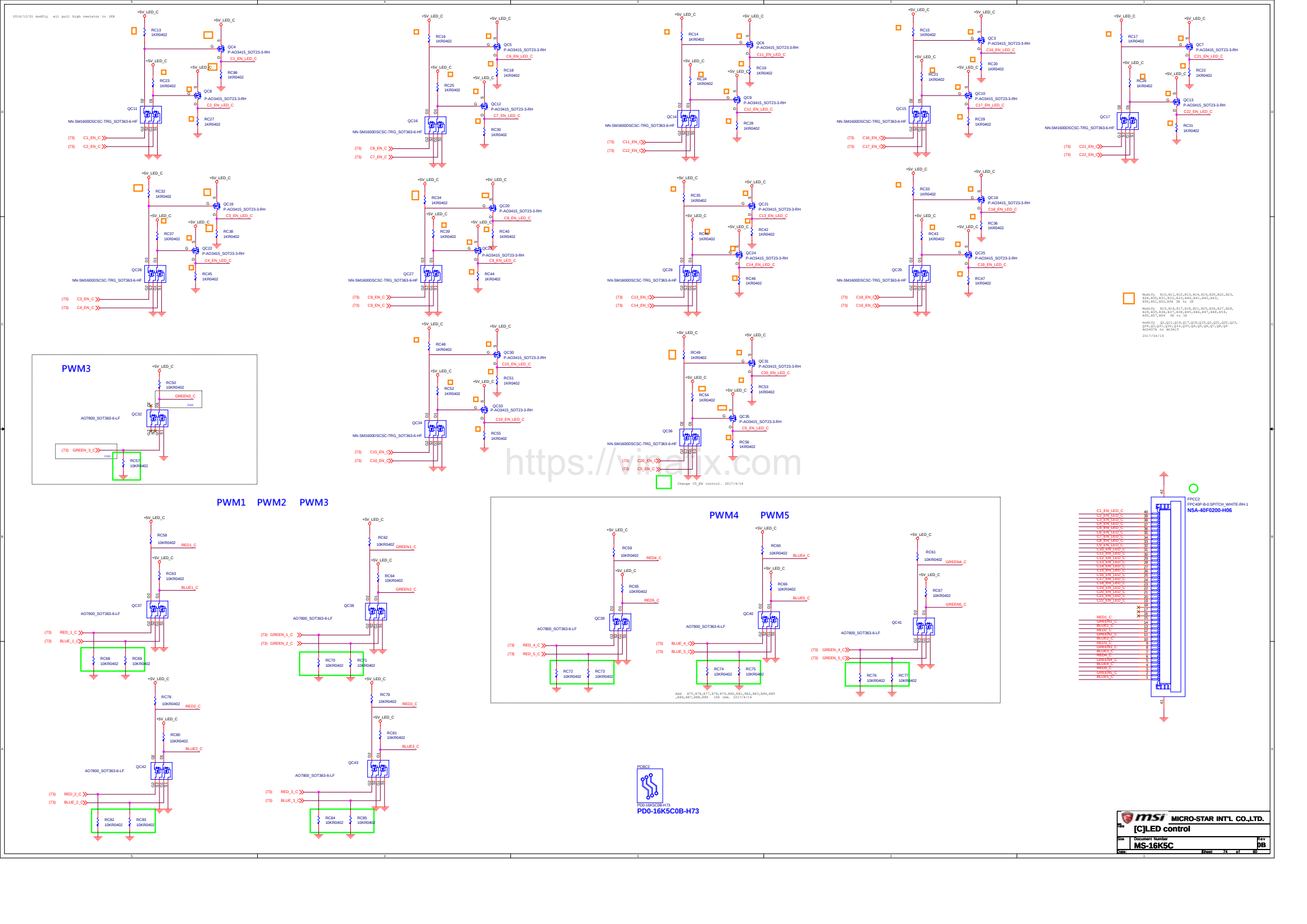
MICRO-STAR INT'L CO.,LTD.

Title: [C]MCU/Matrix/Power

Size | Document Number: MS-16K5C | Rev: 0B

Date: | Sheet 73 of 80



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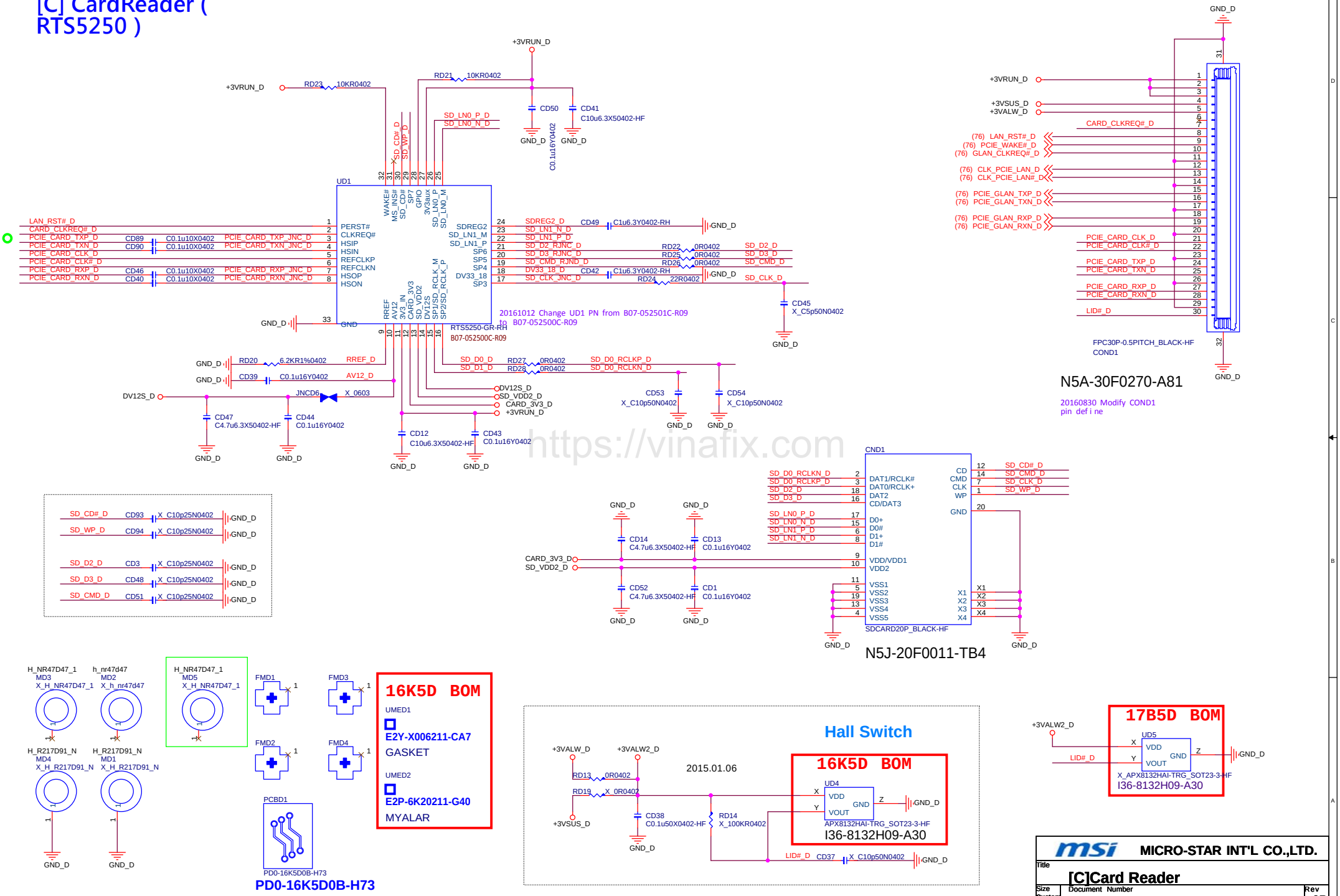
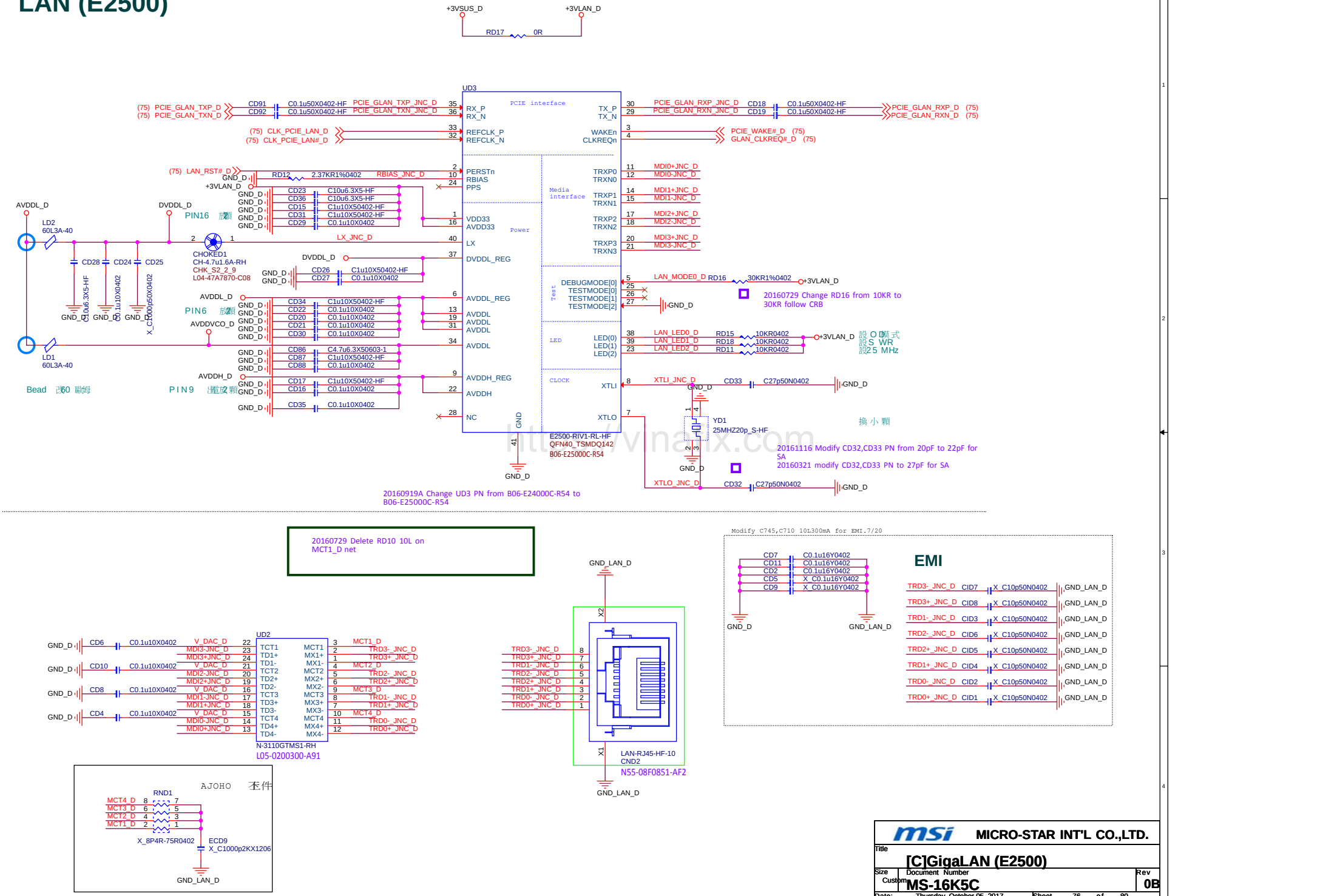
# [C] CardReader ( RTS5250 )




| | |
|---|---|
| MSI | MICRO-STAR INT'L CO.,LTD. |
| Title | [C]Card Reader |
| Size / Custom | Document Number: MS-16K5C |
| Rev | 0B |
| Date: | Friday, October 13, 2017 |
| Sheet | 75 of 80 |

# LAN (E2500)

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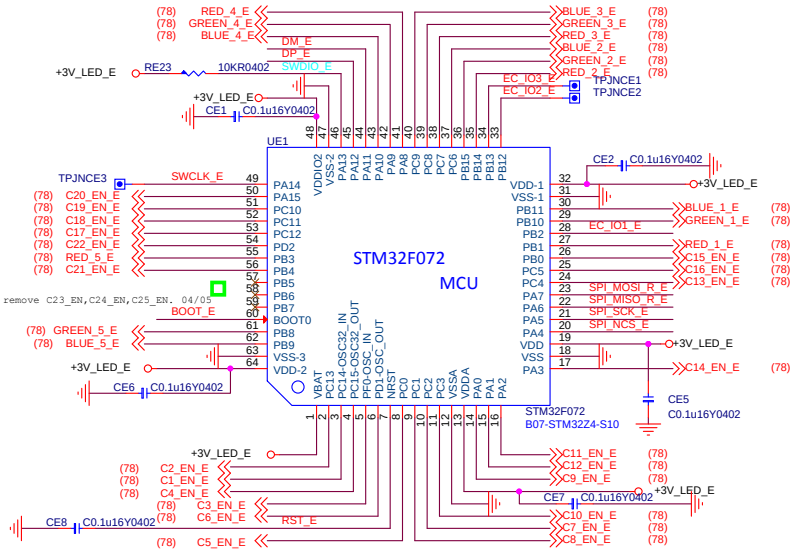
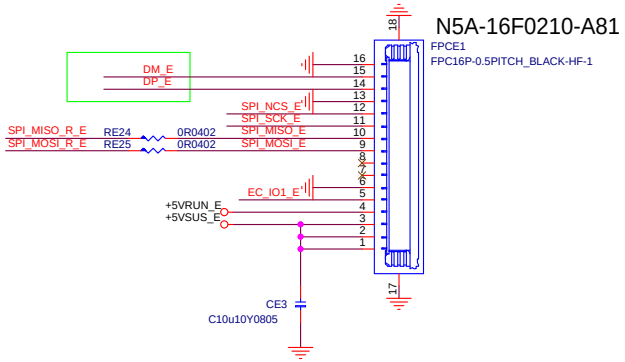
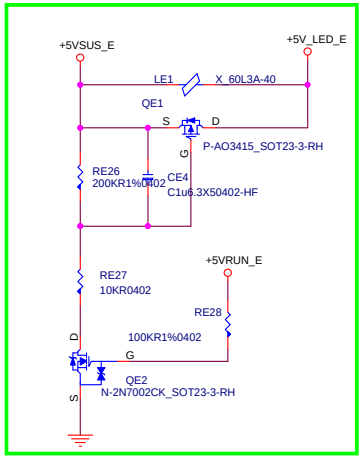
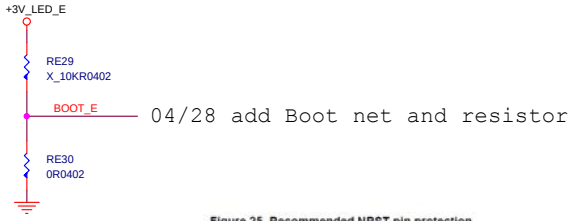
| | | | |
|---|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | | |
| Title | [C]GigaLAN (E2500) | | |
| Size: Custom | Document Number: MS-16K5C | | Rev: 0B |
| Date: Thursday, October 05, 2017 | Sheet 76 of 80 | | |

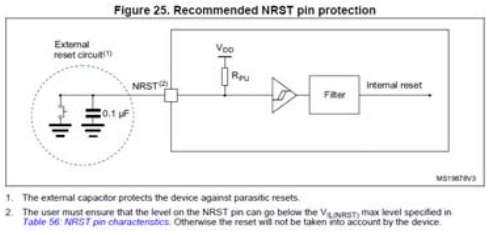


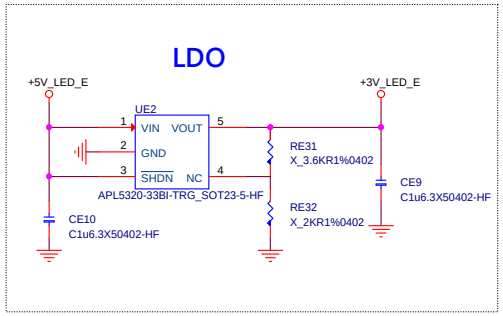




*Confirm Pin 1 position*

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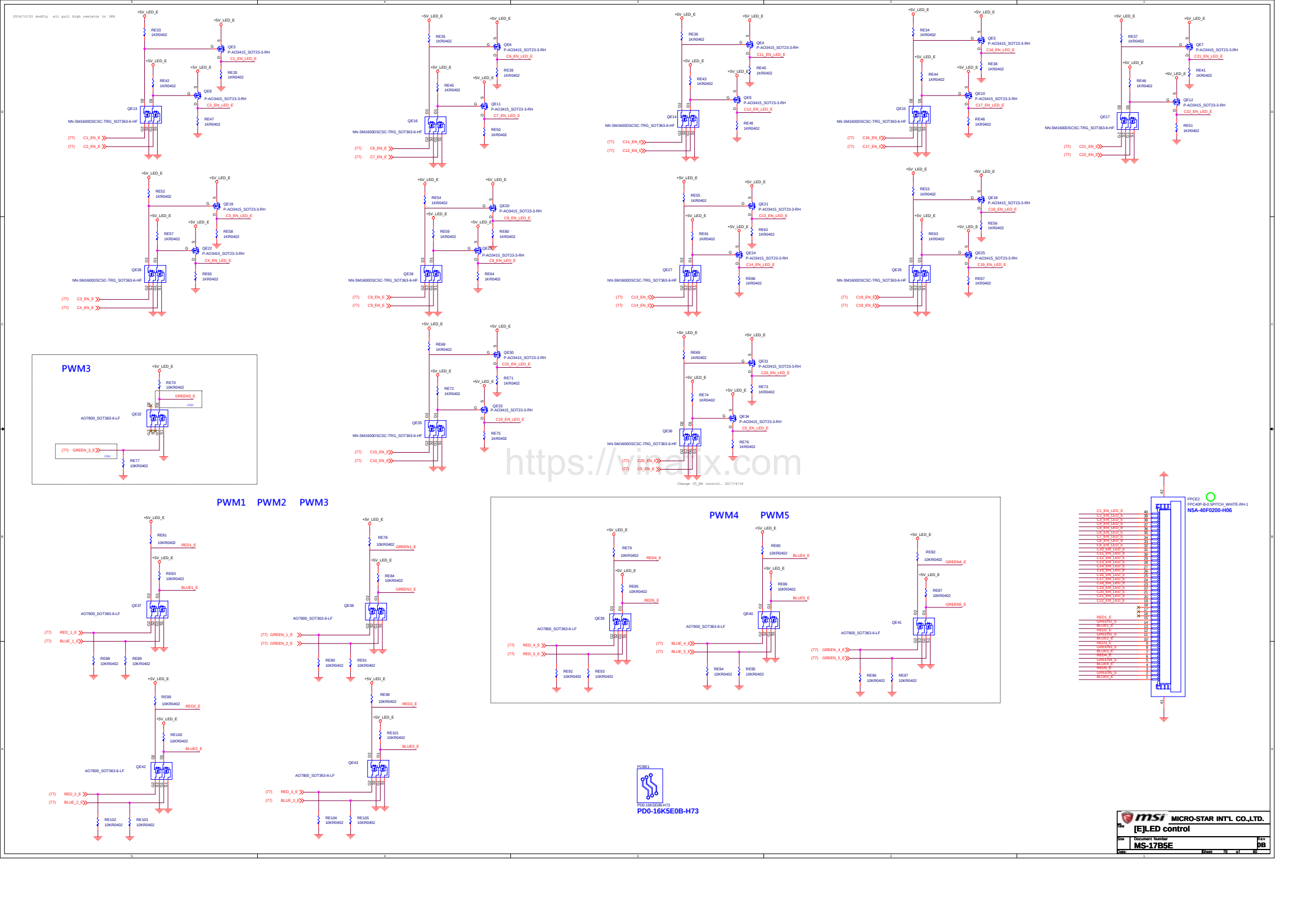
| | | |
|---|---|---|
| Title | MICRO-STAR INT'L CO.,LTD. | |
| | [E]MCU/Matrix/Power | |
| Size | Document Number | Rev |
| | MS-17B5E | 0B |
| Date: | Sheet 77 of 80 | |



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# LED 8051 Controller

F PCB 8/21 增加

C749 and C750 change to 15pF for SA

EPF021J Sink current not enough, only using BSS138 (0.22A)

Chip / Conn

Chip / Conn

Chip / Conn

Chip / Conn

Chip / Conn

解決 K B開關 的問 題

EPF021J

B07-F021J44-EB3

PCBF1

PD0-16K6F0A-H73

PD0-16K5F0B-H73

*AVL : PD0-16K5F0B-T53*

MHF2 X_H_NR118D118

MHF1 X_H_NR118D118

Pin12 & Pin13 have diff branch

FOR FW CHANGE

LED Keyboard CONN

電容擺放位置 需 確 認
INRUCH CURRENT

| LED Keyboard Pin Define | |
|---|---|
| Pin 1 | VCC_G |
| Pin 2 | VCC_R |
| Pin 3 | VCC_B |
| Pin 4 | LED1_B |
| Pin 5 | LED1_R |
| Pin 6 | LED1_G |
| Pin 7 | LED2_B |
| Pin 8 | LED2_R |
| Pin 9 | LED2_G |
| Pin 10 | LED3_B |
| Pin 11 | LED3_R |
| Pin 12 | LED3_G |

FPCF2
FPC12P-0.5PITCH_BLACK-HF-1
N5A-12F0330-A81
掀蓋 式

FPCF1
FPC16P-0.5PITCH_BLACK-HF-1
N5A-16F0210-A81

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MICRO-STAR INT'L CO.,LTD.

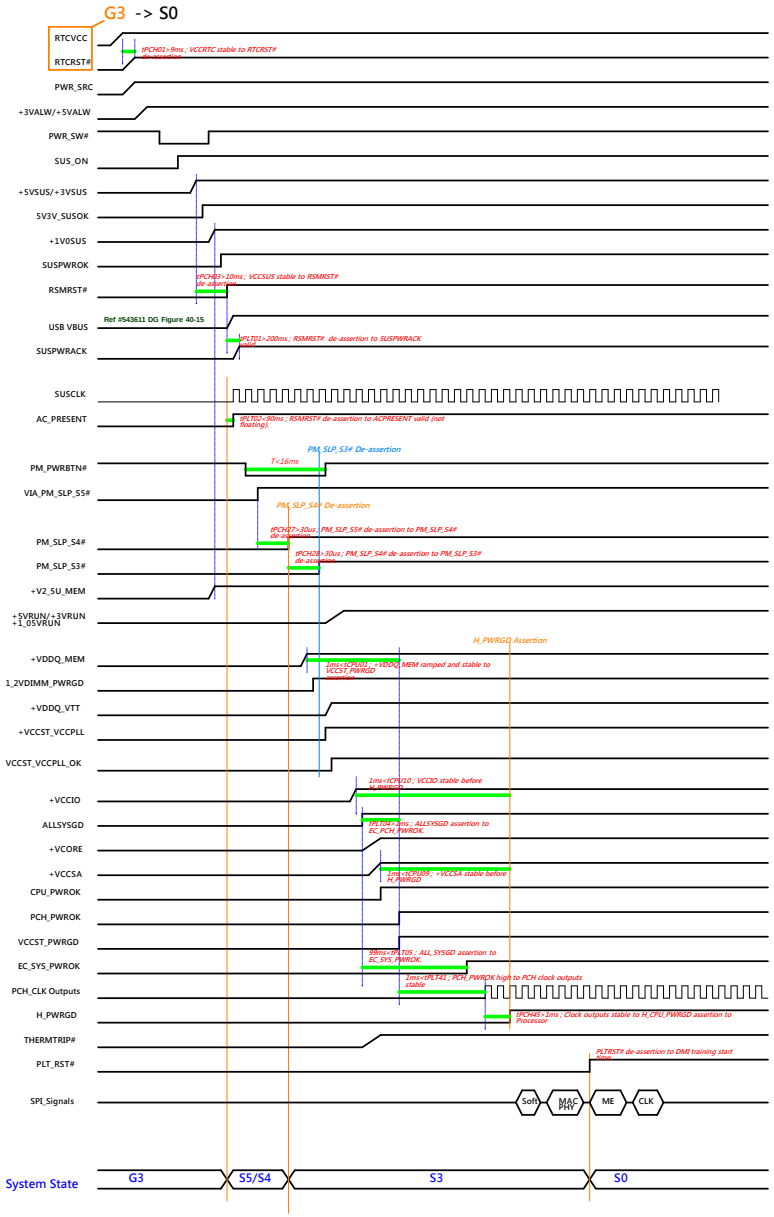
Title: [F] RGB LED K/B control

Size: C | Document Number: MS-16K5F | Rev: 0B

Date: Tuesday, October 03, 2017 | Sheet 79 of 80

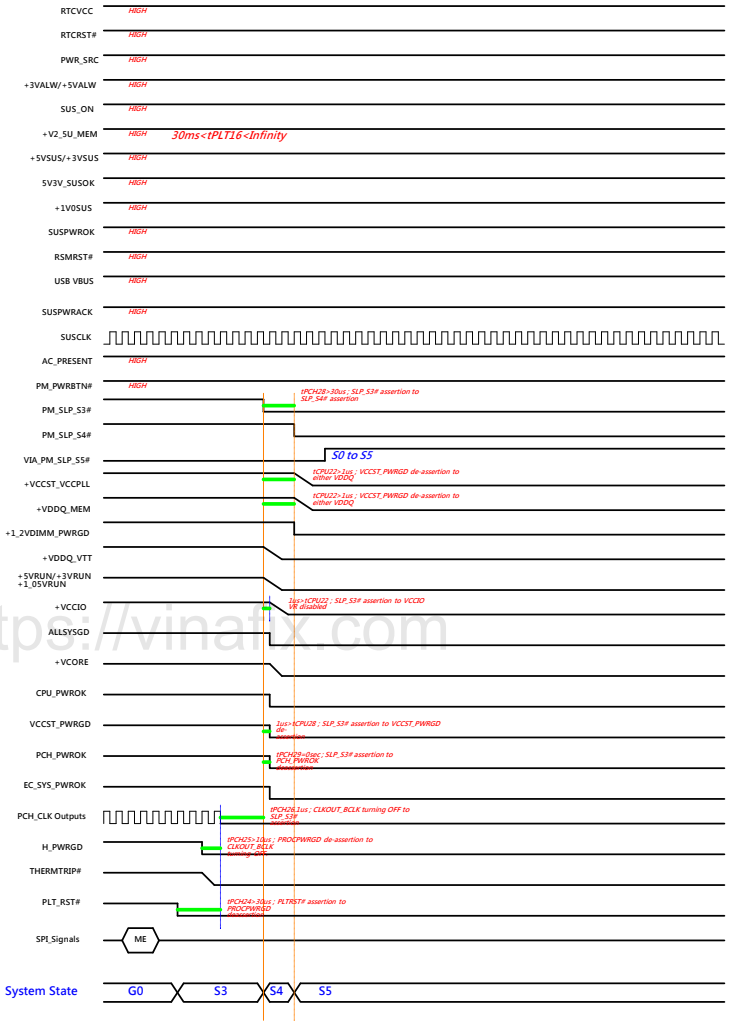
## SKL-S DT Power ON Sequence G3 to S0

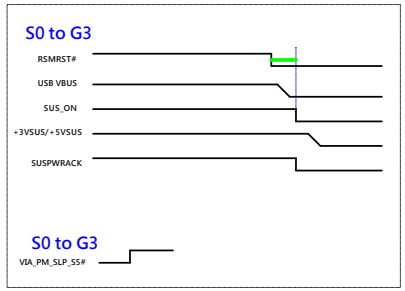
Ref #543611 Chapter40
Figure 40-4. SKL-S Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform]
Table 40-5. Platform Sequencing Timing Parameters




## MS-1813 : SKL-S DT Power Down Sequence S0 to S5

Ref #543611 Chapter40
Figure 40-6. SKL-S Timing Diagram for S0 to G3 [Non-Deep Sx Platform]
Table 40-5. Platform Sequencing Timing Parameters

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| | | |
|---|---|---|
| MICRO-STAR INT'L CO.,LTD. | | |
| File: Power on Sequence | | |
| Size: | Document Number: MS-16K5 | Rev: 0B |
| Date: Tuesday, October 03, 2017 | Sheet 80 of 80 | |